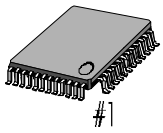
INTRODUCTION

The S5C7214X01 is a timing control IC for generating timing signals & pulses for B/W sync signals which are required for camera systems using monochrome CCD Image sensors.

48-QFP-0707



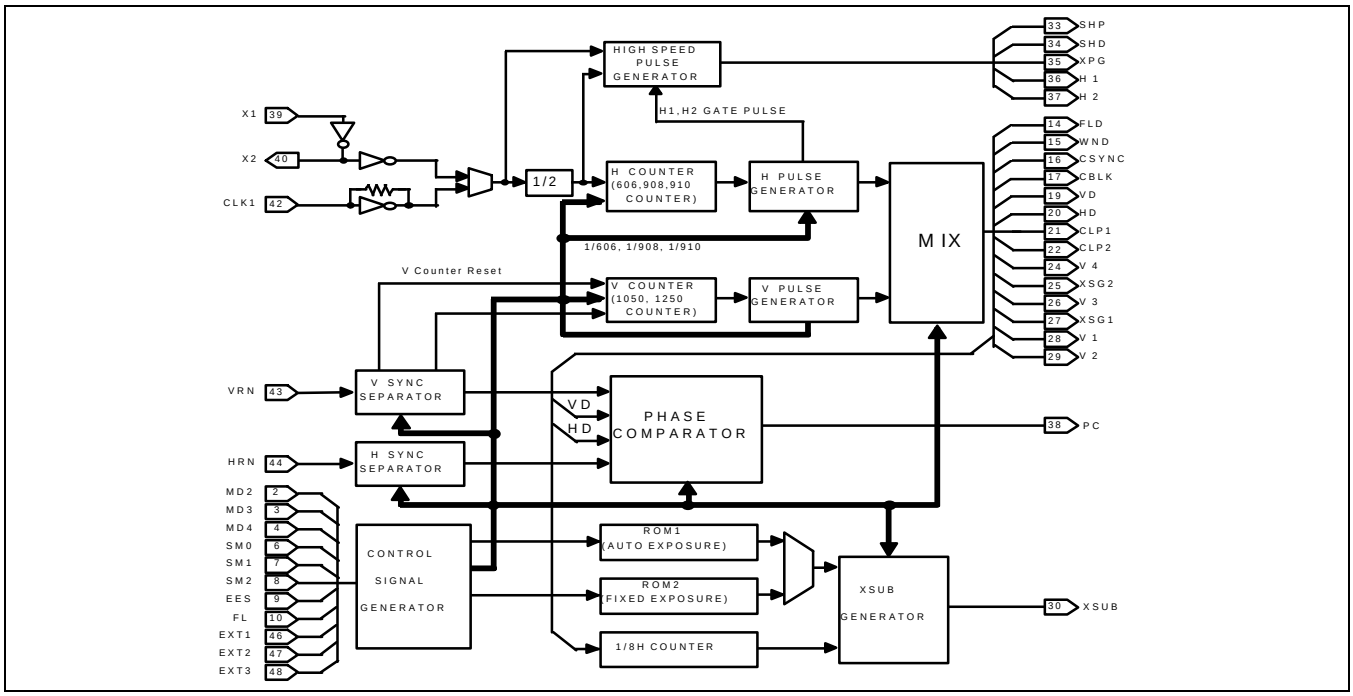
FEATURES

- EIA / CCIR STANDARDS TIMING MODE
- HI-BAND / NORMAL TIMING MODE
- FRAME / FIELD ACCUMULATION MODE
- INTERLACE / NON - INTERLACE MODE
- EXTERNAL SYNCHRONIZATION MODE
- ELECTRONIC IRIS (ELECTRONIC SHUTTER)
- SYNC SIGNAL GENERATION
- OSCILLATION FREQUENCY :
  EIA NORMAL MODE : 19.06992 MHz
  CCIR NORMAL MODE : 18.93750 MHz
  EIA HI-BAND MODE : 28.63636 MHz
  CCIR HI-BAND MODE : 28.37500 MHz

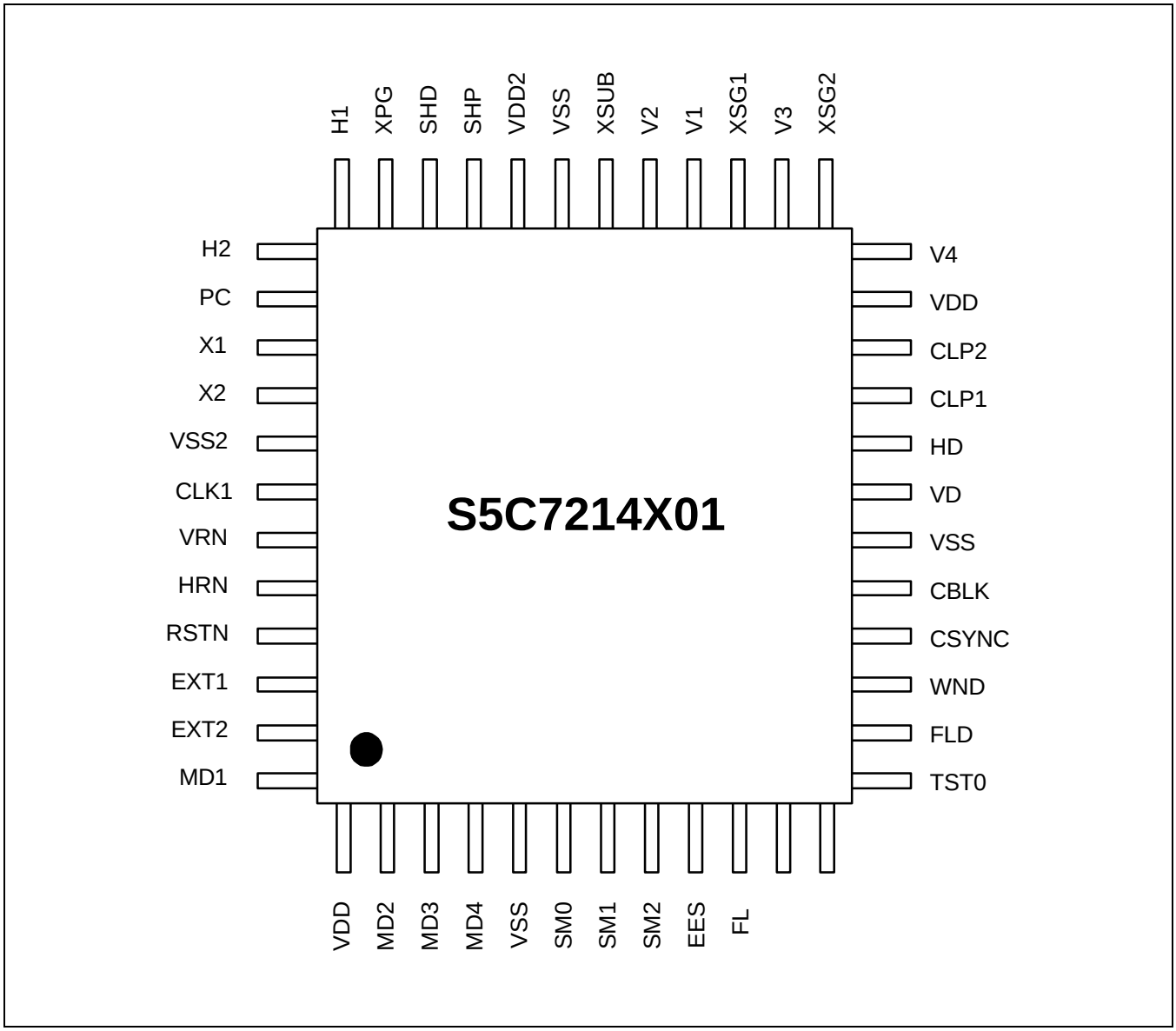
ORDERING INFORMATION

Device	Package	Operating
S5C7214X01-E0R0	48-QFP-0707	-20 °C – 75 °C

BLOCK DIAGRAM



PIN CONFIGURATION



SAMSUNG ELECTRONICS

PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Description
1	VDD	-	Power Supply
2	MD2	I	Mode Switching; HI-Band: High, Normal: Low (with Pull-down)
3	MD3	I	Mode Switching; Non - Interlace: High, Interlace: Low (with Pull-down)
4	MD4	I	Mode Switching; Frame : High, Field: Low (with Pull-down)
5	VSS	-	Ground
6	SM0	I	Shutter Speed Control (with Pull-down)
7	SM1	I	Shutter Speed Control (with Pull-down)
8	SM2	I	Shutter Speed Control (with Pull-down)
9	EES	I	Electronic Shutter Mode; Auto Mode: High, Fixed Mode: Low (with Pull-down)
10	FL	I	Flickerless Shutter Mode; Flickerless Mode: High (with Pull-down)
11	TST2	I	Test Mode Select 2 (with Pull-down)
12	TST1	I	Test Mode Select 1 (with Pull-down)
13	TST0	I	Test Mode Select 0 (with Pull-down)
14	FLD	O	Field Separation Pulse
15	WND	O	Window Pulse
16	CSYNC	O	Composite Sync Pulse
17	CBLK	O	Composite Blank Pulse
18	VSS	-	Ground
19	VD	O	Vertical Drive Pulse
20	HD	O	Horizontal Drive Pulse
21	CLP1	O	Clamp Pulse 1
22	CLP2	O	Clamp Pulse 2
23	VDD	-	Power Supply
24	V4	O	CCD Vertical Register Drive Pulse 4

PIN DESCRIPTION (Continued)

Pin No.	Pin Name	I/O	Pin Description
25	XSG2	O	CCD Sensor Read Out Pulse 2
26	V3	O	CCD Vertical Register Drive Pulse 3
27	XSG1	O	CCD Sensor Read Out Pulse 1
28	V1	O	CCD Vertical Register Drive Pulse 1
29	V2	O	CCD Vertical Register Drive Pulse 2
30	XSUB	O	CCD Discharge Pulse
31	VSS	-	Ground
32	VDD2	-	Power Supply 2
33	SHP	O	Precharge Sample & Hold Pulse
34	SHD	O	Data Sample & Hold Pulse
35	XPG	O	CCD Reset Gate Pulse
36	H1	O	CCD Horizontal Register Drive Pulse
37	H2	O	CCD Horizontal Register Drive Pulse
38	PC	O	Phase Comparator Output
39	X1	I	Oscillator Input
40	X2	O	Oscillator Output
41	VSS2	-	Ground 2
42	CLKI	I	Clock Input For EXT. Sync Mode
43	VRN	I	Vertical PLL Reference For External Sync Mode (Schmitt Pull-up)
44	HRN	I	Horizontal PLL Reference For External Sync Mode (Schmitt Pull-up)
45	RSTN	I	System Initialization Pulse (Schmitt Pull- up)
46	EXT1	I	External Sync Mode Select (with Pull-down)
47	EXT2	I	External Sync Mode Select (with Pull-down)
48	MD1	I	Mode Switching; CCIR: High, EIA: Low (with Pull-down)

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Parameter	Symbol	Condition	Unit
Supply Voltage	V_{DD}	V_{SS} - 0.3 – + 7.0	V
Input Voltage	V_I	V_{SS} - 0.3 – V_{DD} + 0.3	V
Output Voltage	V_O	V_{SS} - 0.3 – V_{DD} + 0.3	V
Operating Temp.	Topr	0 – + 70	°C
Storage Temp.	Tstr	- 40 – + 125	°C
Latch-up Current	I_{LU}	100	mA

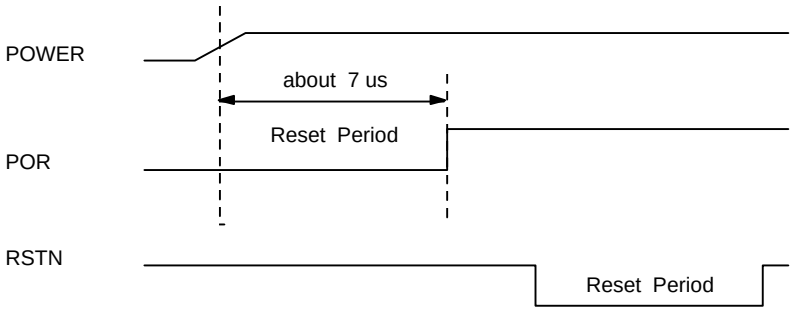
DC CHARACTERISTICS (Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	4.75	5.00	5.25	V
Input voltage 1 (Normal input,	$V_{IH\ 1}$	CMOS Level Interface	$0.7V_{DD}$	-	-	V
except Pin 40, 43, 44, 45)	$V_{IL\ 1}$	CMOS Level Interface	-	-	$0.3V_{DD}$	V
Input voltage 2 (Pin 43, 44, 45)	V_{IH2}	CMOS Level Schmitt trigger	$0.8V_{DD}$	-	-	V
	V_{IL2}	CMOS Level Schmitt trigger	-	-	$0.2V_{DD}$	V
Input Current 1(With pull-down)	I_{IH1}	$V_I = V_{DD}$	50	-	200	uA
	I_{IL1}	$V_I = V_{SS}$	-10	-	10	uA
Input Current 2	I_{IH2}	$V_I = V_{DD}$	-10	-	10	uA
(With pull-up: Pin 43, 44, 45)	I_{IL2}	$V_I = V_{SS}$	-200	-	-50	uA
Input Current 3	I_{IH3}	$V_I = V_{DD}$	-40	-	40	uA
(Normal Input: Pin 42)	I_{IL3}	$V_I = V_{SS}$	-40	-	40	uA
Output voltage 1(Normal output,	V_{OH1}	I_{OH} = -2mA	2.4	-	-	V
except 33, 34, 35, 36, 37, 40)	V_{OL1}	I_{OL} = 2mA	-	-	0.4	V
Output voltage 2 (Pin 33, 34, 35)	V_{OH2}	I_{OH} = -4mA	2.4	-	-	V
	V_{OL2}	I_{OL} = 4mA	-	-	0.4	V
Output voltage 3 (Pin 36, 37)	V_{OH3}	I_{OH} = -16mA	2.4	-	-	V
	V_{OL3}	I_{OL} = 16mA	-	-	0.4	V
Operating current	I_{DD}	V_{DD} = 5.25 V	-	25	50	mA
Static current	I_{ST}	V_{DD} = 5.25 V	-	420	-	uA

OPERATION

INTERNAL RESET OPERATION

- Including power on reset. (Typ. 7us)
- RSTN low active reset at the internal mode



EXTERNAL SYNCHRONIZATION OPERATION

EXT 1	EXT 2	MODE
0	0	Internal Sync. Mode
0	1	External Composite Sync. Mode
1	0	Line Lock Sync. Mode
1	1	Separate Sync. Mode

HD PHASE SELECTION

TST 2	TST 1	TST0	MODE
0	0	0	Normal HD
1	1	1	Reversed HD
ELSE			Reversed

ELECTRONIC SHUTTER

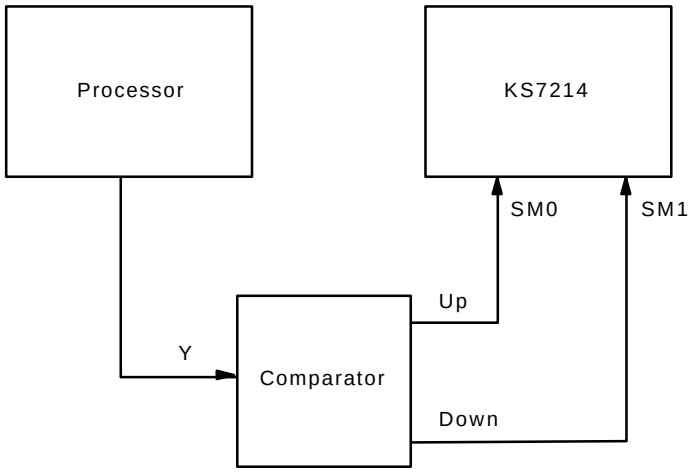
There are two electronic shutter modes in S5C7214X01.
One is a Fixed Iris mode that controls shutter speed through parallel interface with the external pin. The other is an Auto Iris mode that controls the electronic Iris automatically by detecting the amount of light of current objects from the signal process IC.

FIXED SHUTTER MODE

MD1	FL	SM2	SM1	SM0	SHUTTER SPEED	
					STEP	REAL
L	L	L	L	L	1/60	1/60
L	L	L	L	H	1/250	1/251
L	L	L	H	L	1/500	1/513
L	L	L	H	H	1/1000	1/1006
L	L	H	L	L	1/2000	1/1936
L	L	H	L	H	1/5000	1/5034
L	L	H	H	L	1/10000	1/10489
L	L	H	H	H	1/30000	1/31469
L	H	X	X	X	1/100 *	1/101
H	L	L	L	L	1/50	1/50
H	L	L	L	H	1/250	1/249
H	L	L	H	L	1/500	1/510
H	L	L	H	H	1/1000	1/999
H	L	H	L	L	1/2000	1/1923
H	L	H	L	H	1/5000	1/5000
H	L	H	H	L	1/10000	1/10416
H	L	H	H	H	1/30000	1/31249
H	H	X	X	X	1/120 *	1/120

* FLICKERLESS MODE

AUTO SHUTTER MODE



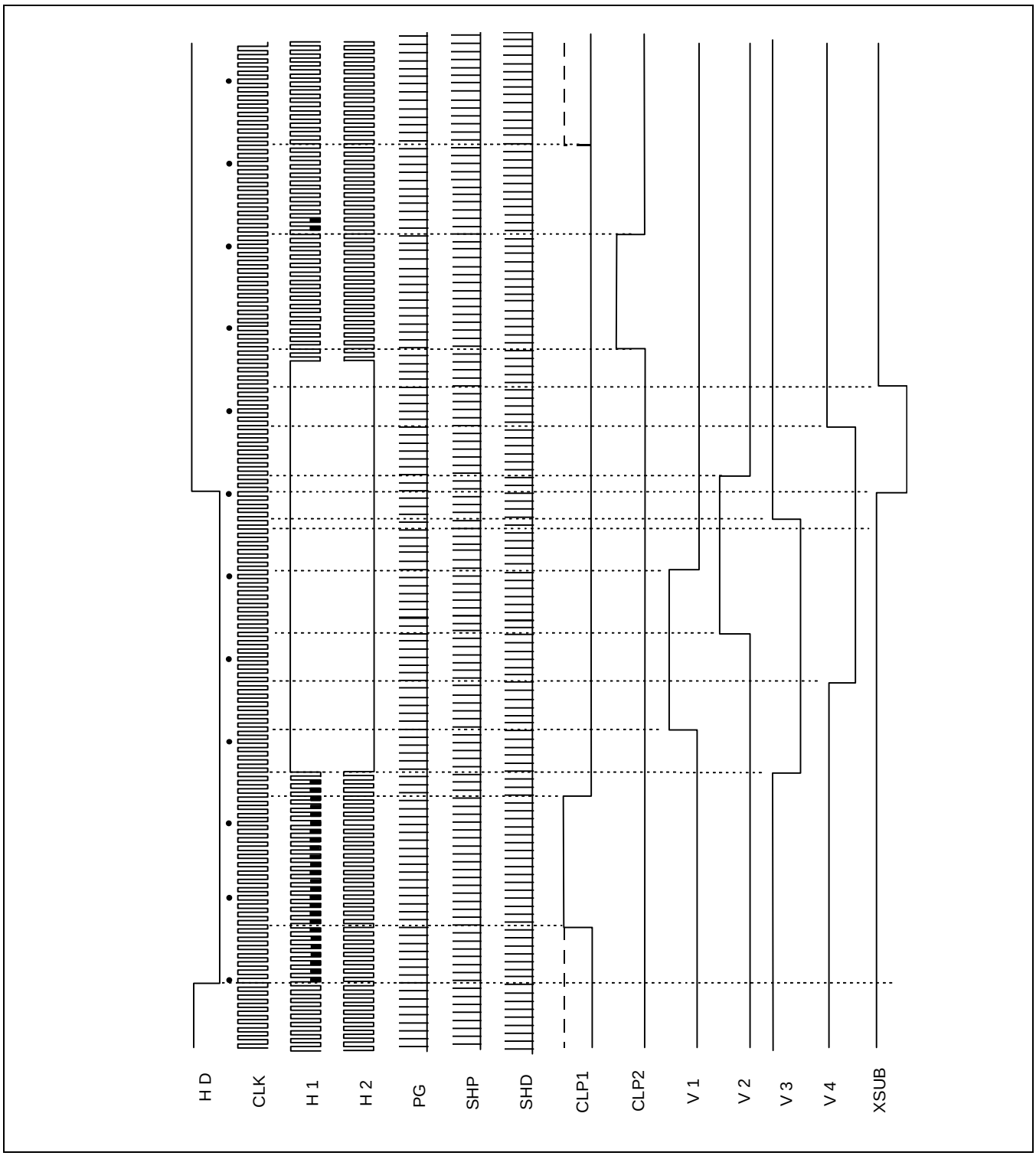
SM1	SM0	Auto Shutter Mode
0	0	Shutter Speed Hold
0	1	Shutter Speed UP
1	0	Shutter Speed DOWN
1	1	Shutter Speed Hold

< Auto shutter application >

NO	Step Period	EIA		CCIR	
		Step	Shutter Speed	Step	Shutter Speed
1	7H	8	1/60 — 1/76	8	1/50 — 1/75
2	5H	7	1/77 — 1/91	7	1/76 — 1/91
3	4H	9	1/92 — 1/116	9	1/92 — 1/115
4	3H	12	1/117 — 1/157	12	1/116 — 1/156
5	2H	18	1/158 — 1/247	18	1/157 — 1/245
6	1H	50	1/248 — 1/1154	50	1/246 — 1/1146
7	1 / 2H	18	1/1155 — 1/3402	18	1/1147 — 1/3378
8	1 / 4H	12	1/3403 — 1/9682	12	1/3379 — 1/9615
9	1 / 8H	11	1/9683 — 1/125875	11	1/9616 — 1/124999

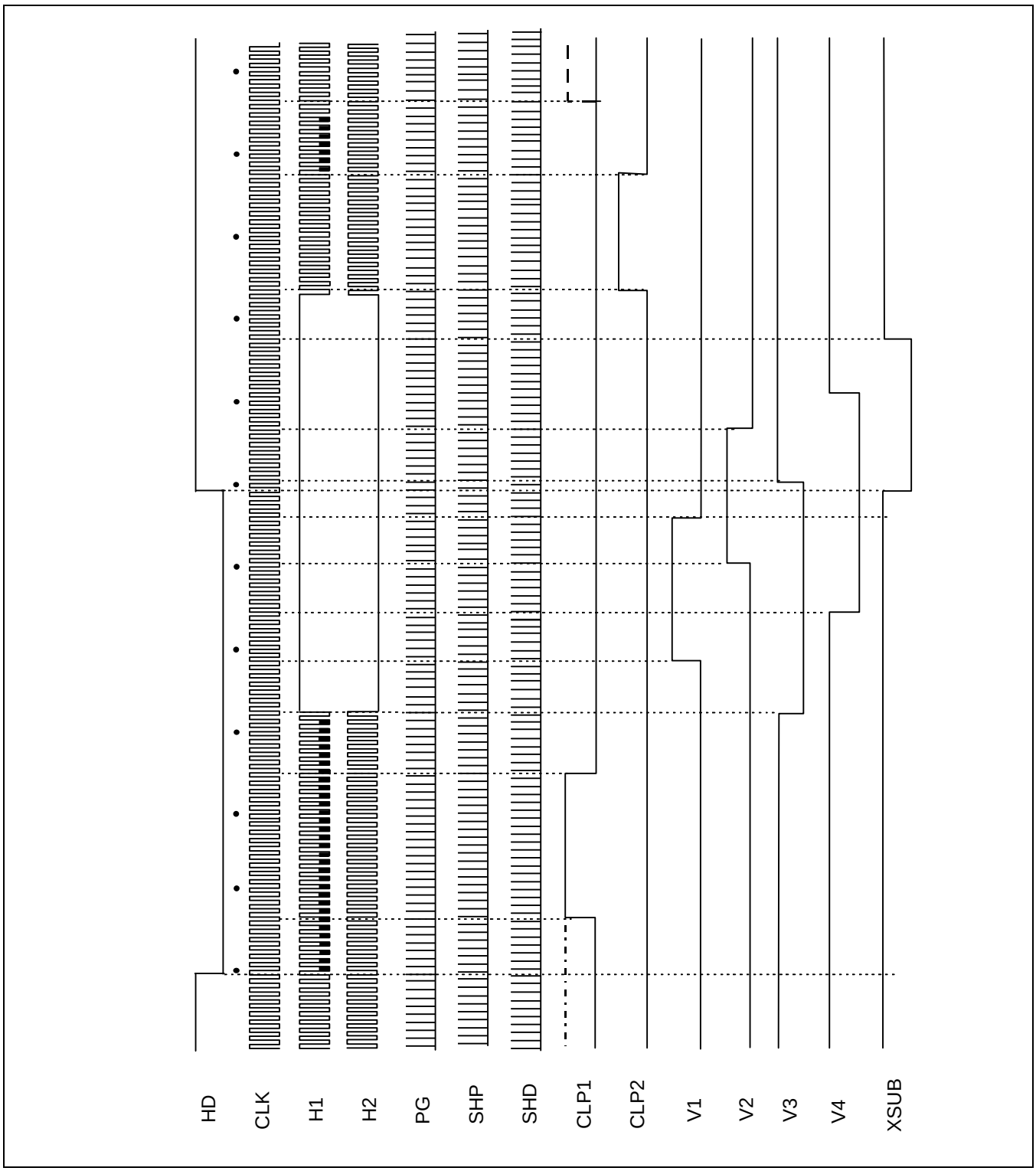
< Auto shutter speed table >

HORIZONTAL TIMING CHART FOR EIA NORMAL

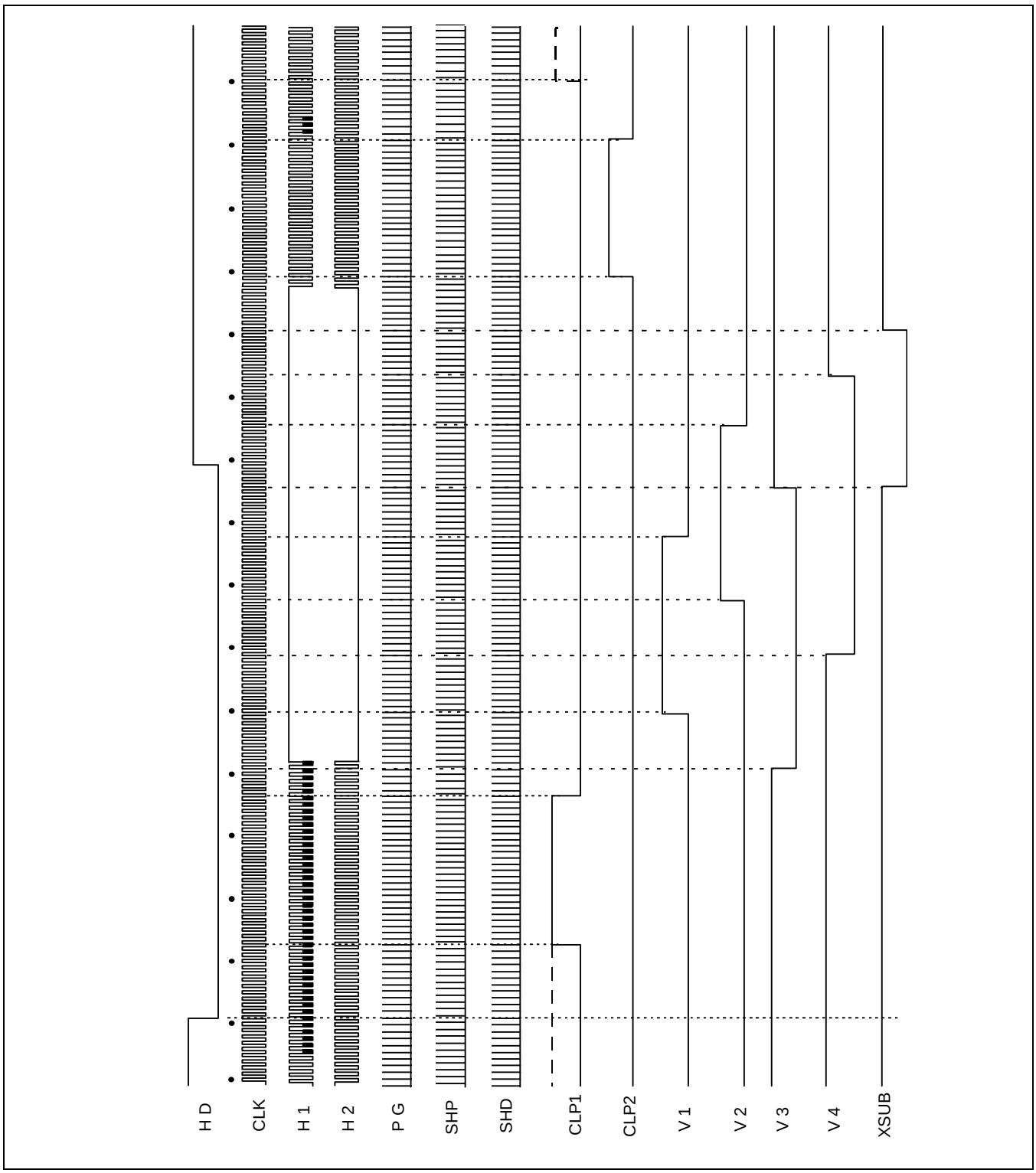


SAMSUNG ELECTRONICS

HORIZONTAL TIMING CHART FOR CCIR NORMAL

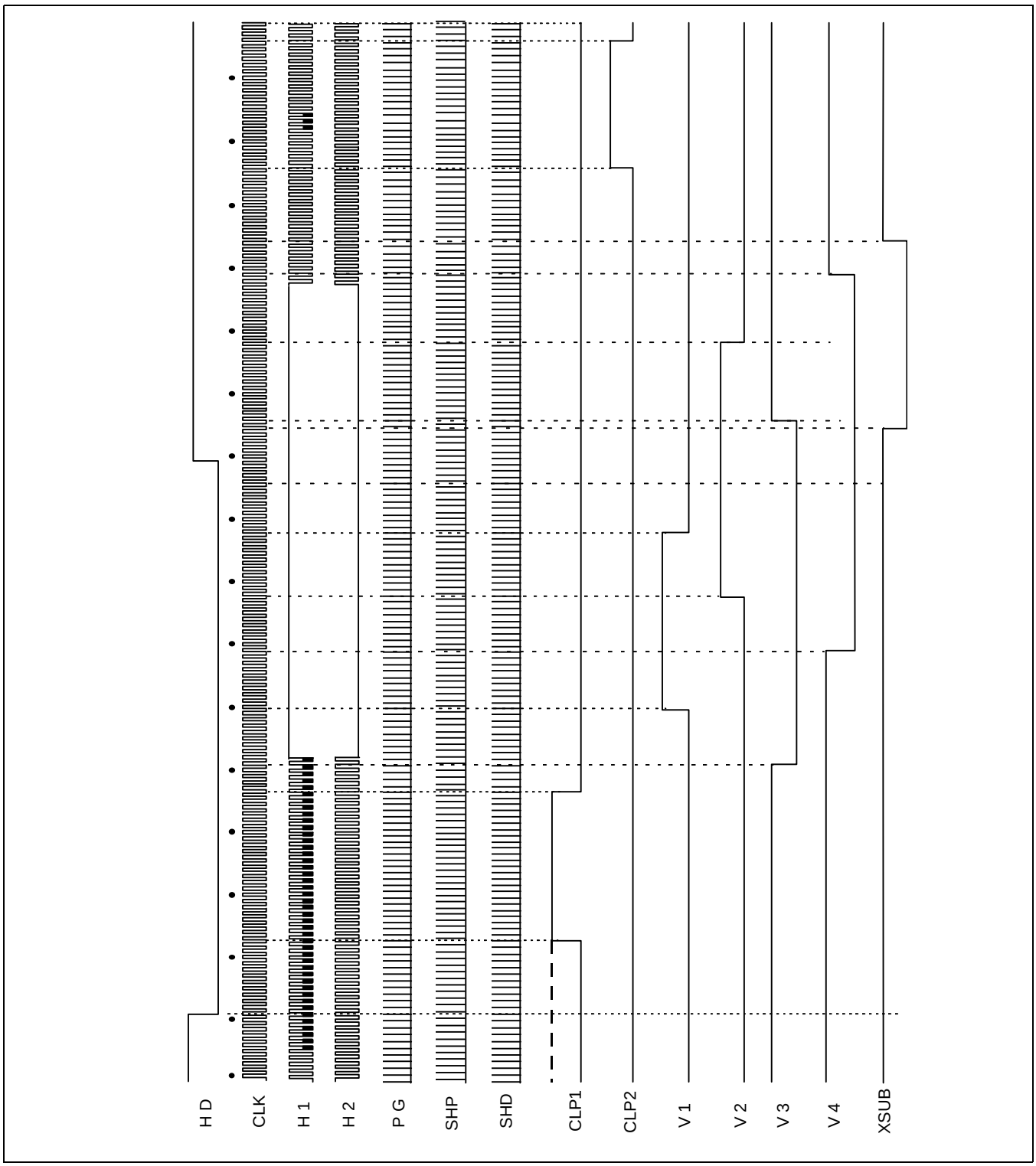


HORIZONTAL TIMING CHART FOR EIA Hi- 8

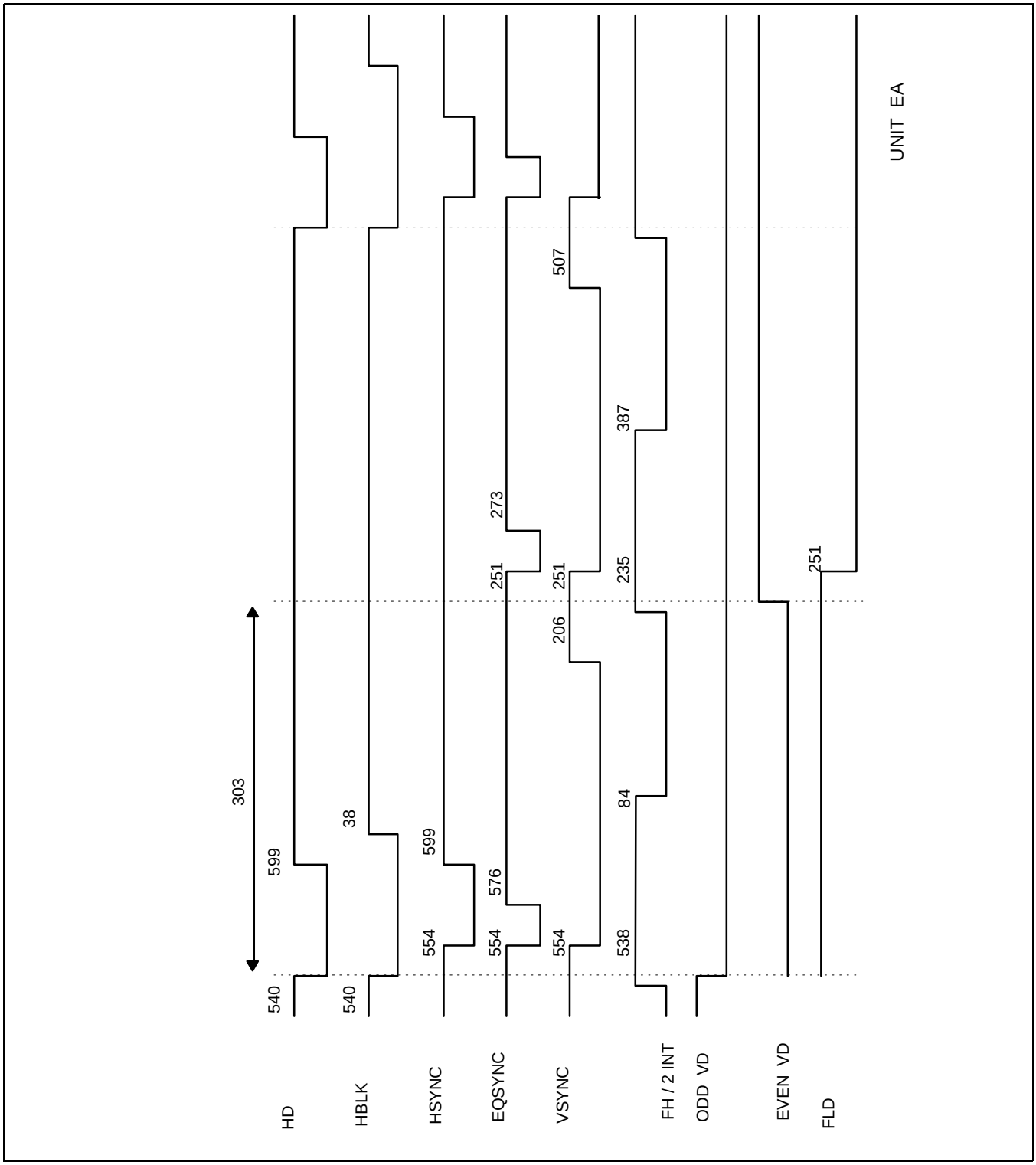


SAMSUNG ELECTRONICS

HORIZONTAL TIMING CHART FOR CCIR Hi- 8

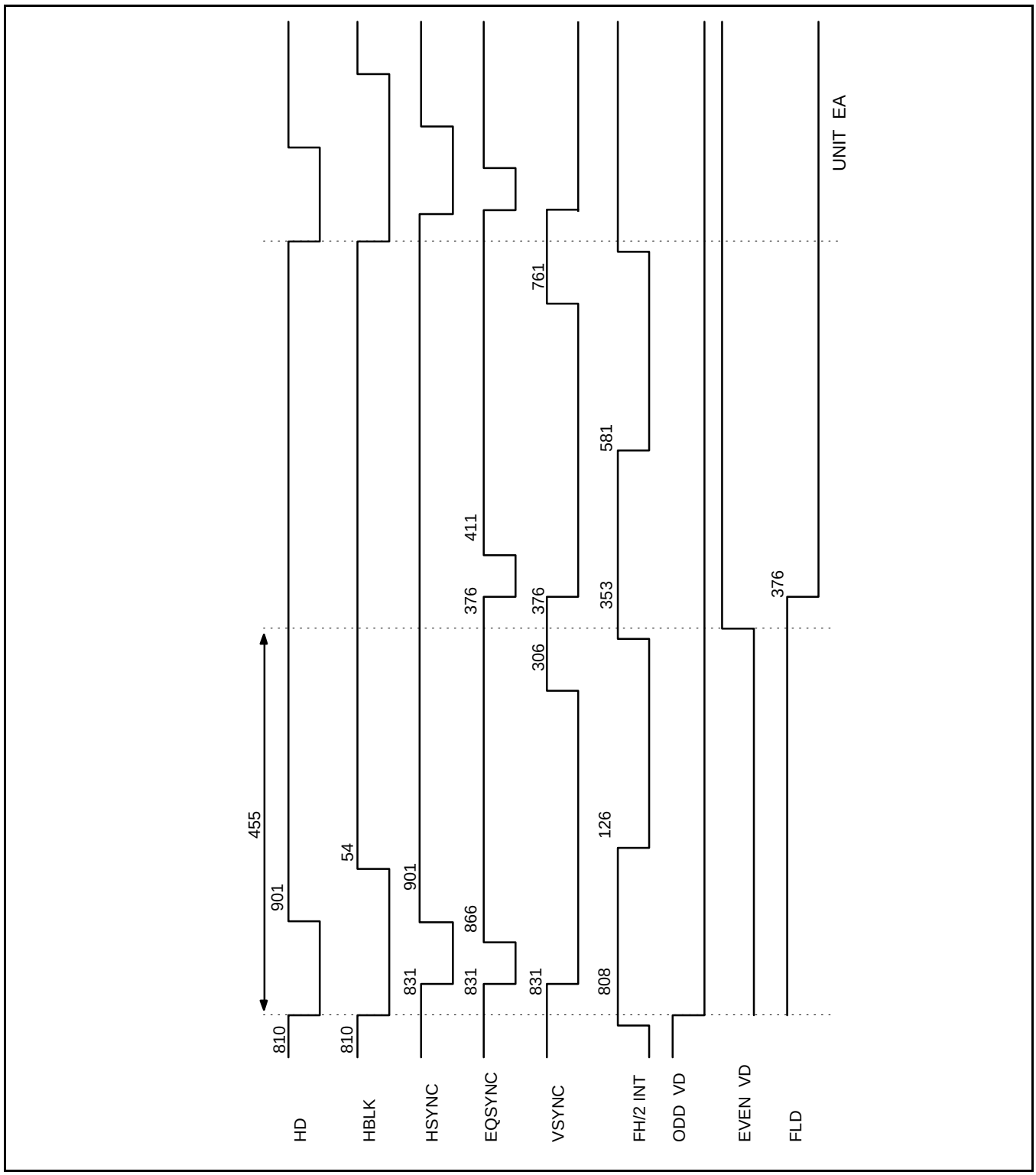


HORIZONTAL TIMING CHART FOR EIA NORMAL

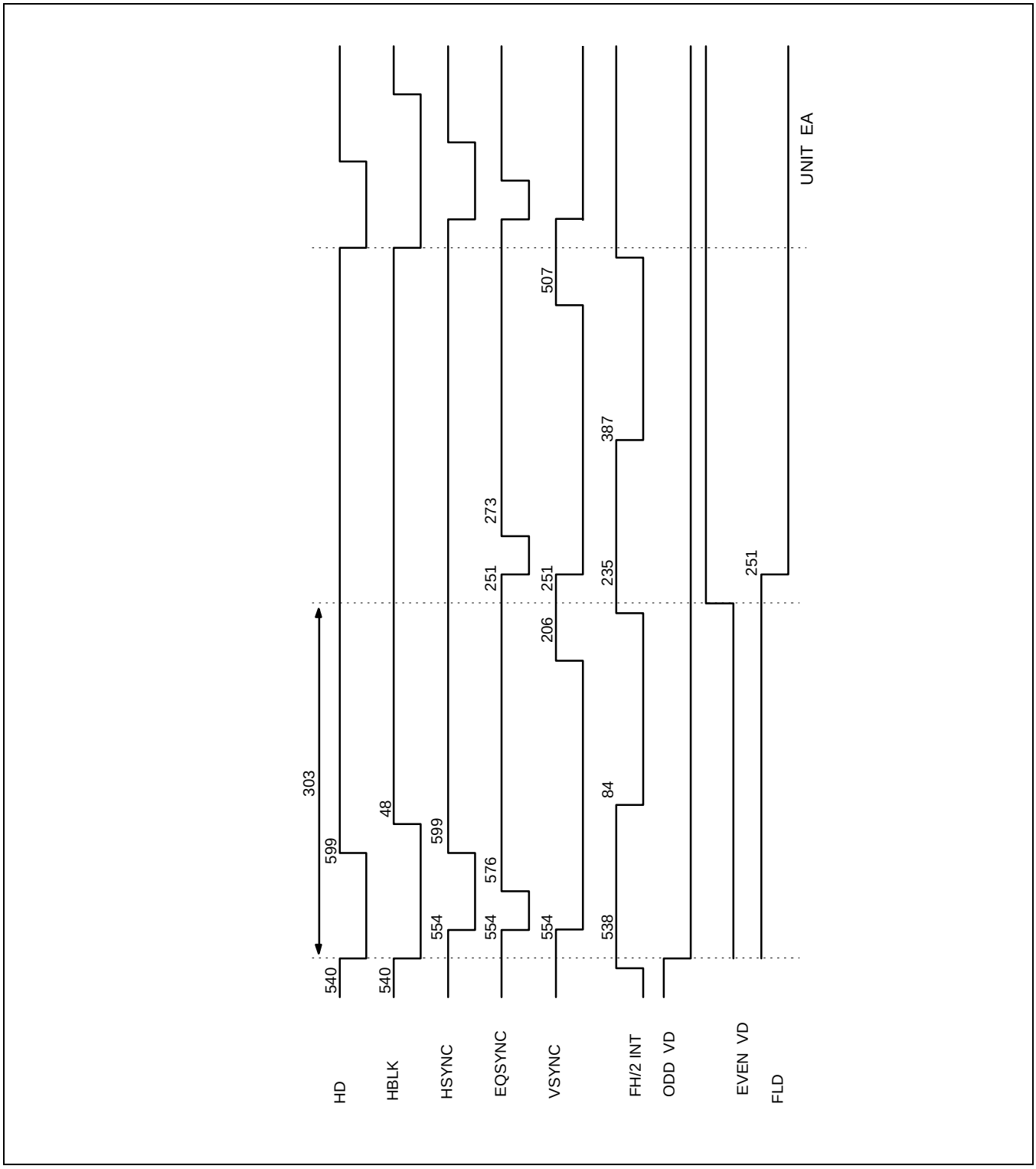


SAMSUNG ELECTRONICS

HORIZONTAL TIMING CHART FOR EIA Hi- 8

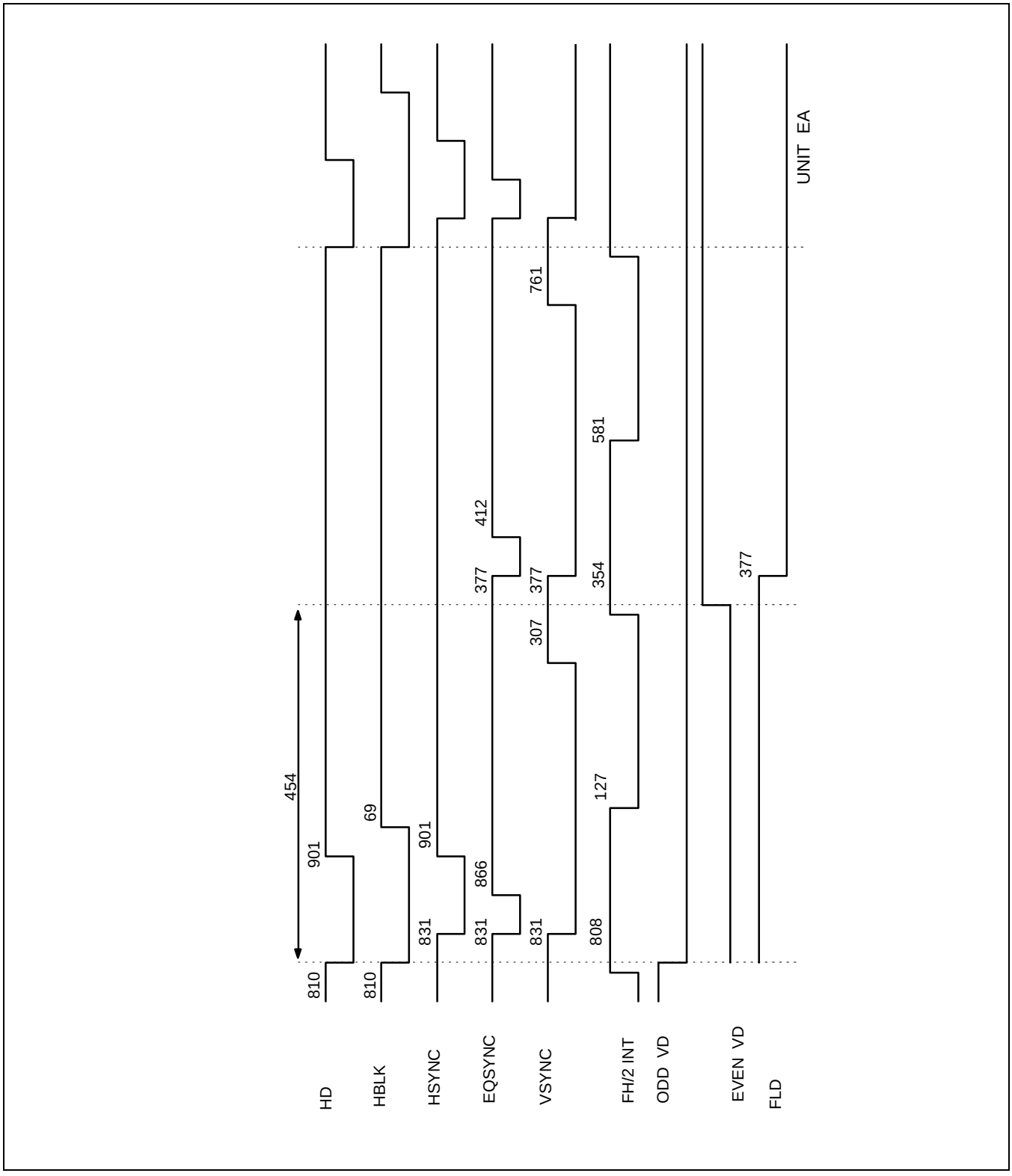


HORIZONTAL TIMING CHART FOR CCIR NORMAL

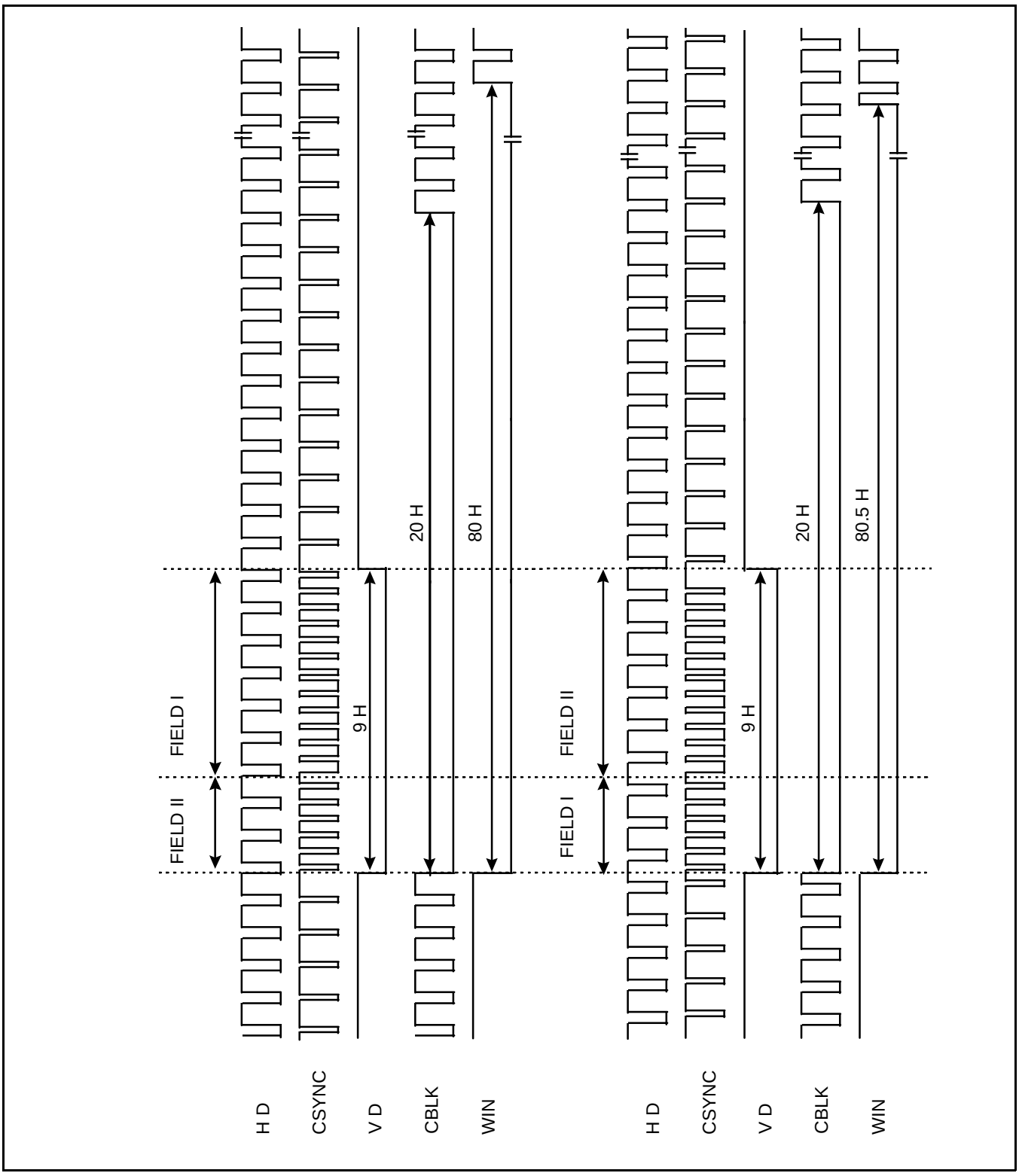


SAMSUNG ELECTRONICS

HORIZONTAL TIMING CHART FOR CCIR Hi- 8

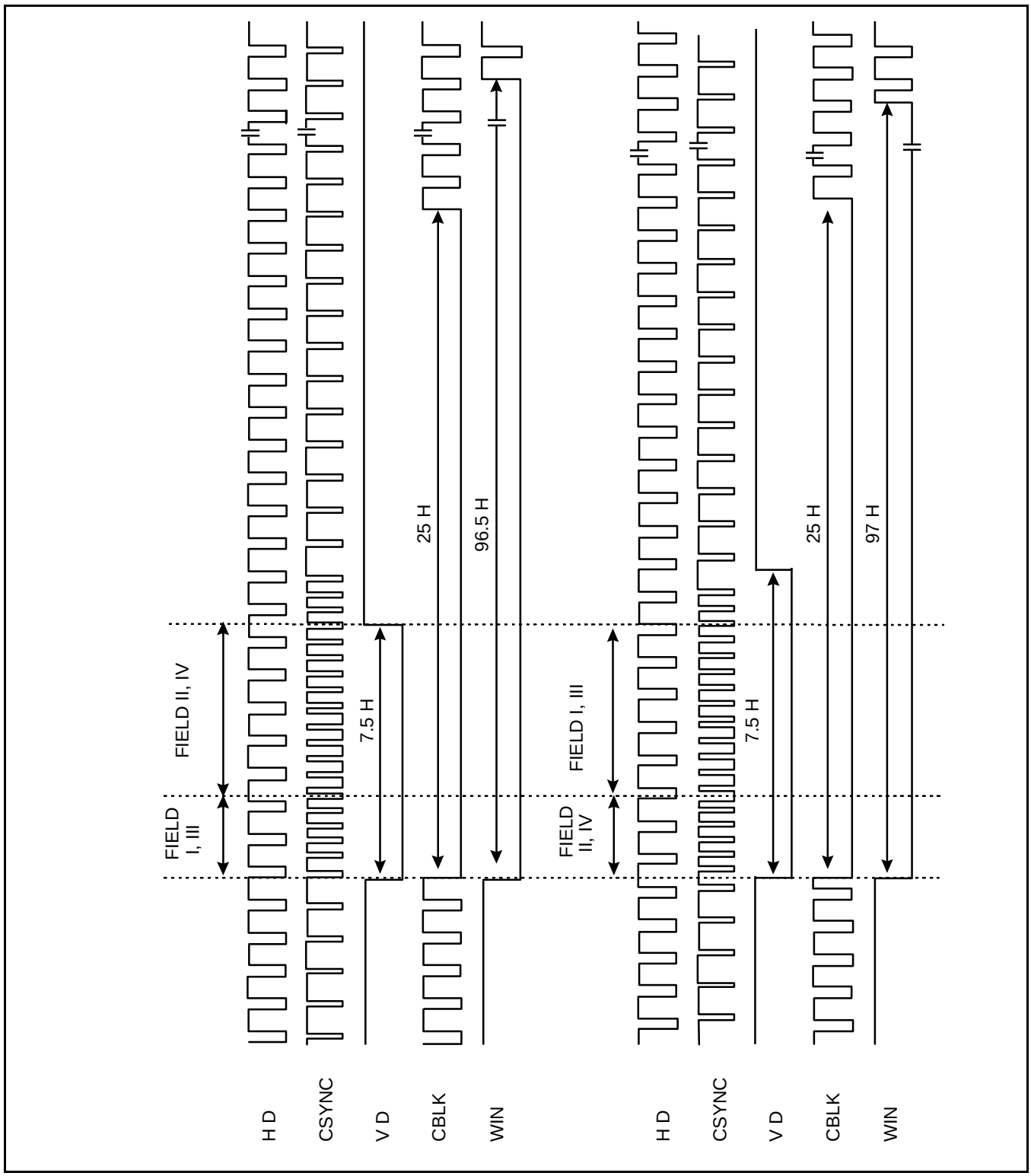


VERTICAL TIMING CHART FOR EIA

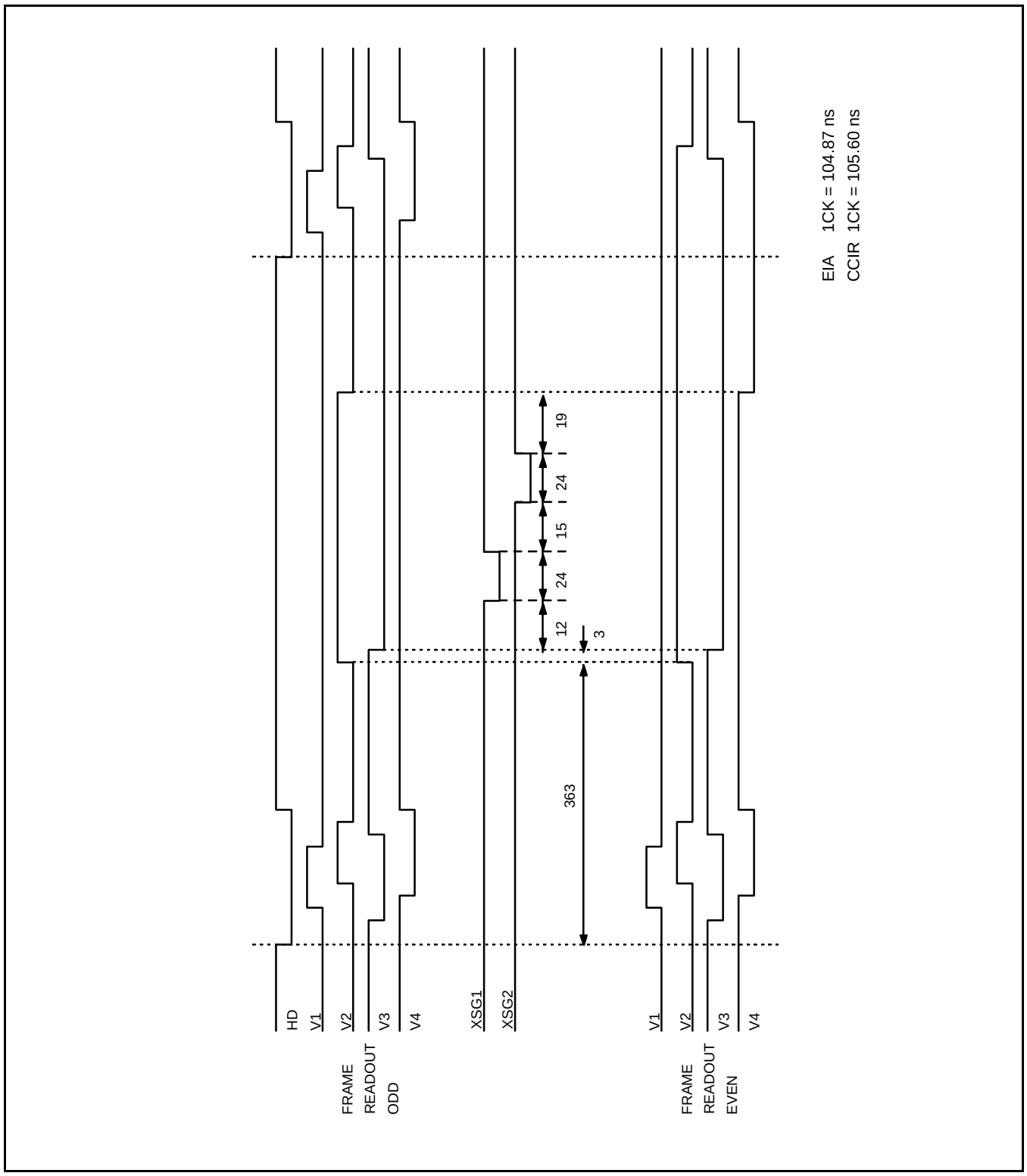


SAMSUNG ELECTRONICS

VERTICAL TIMING CHART FOR CCIR

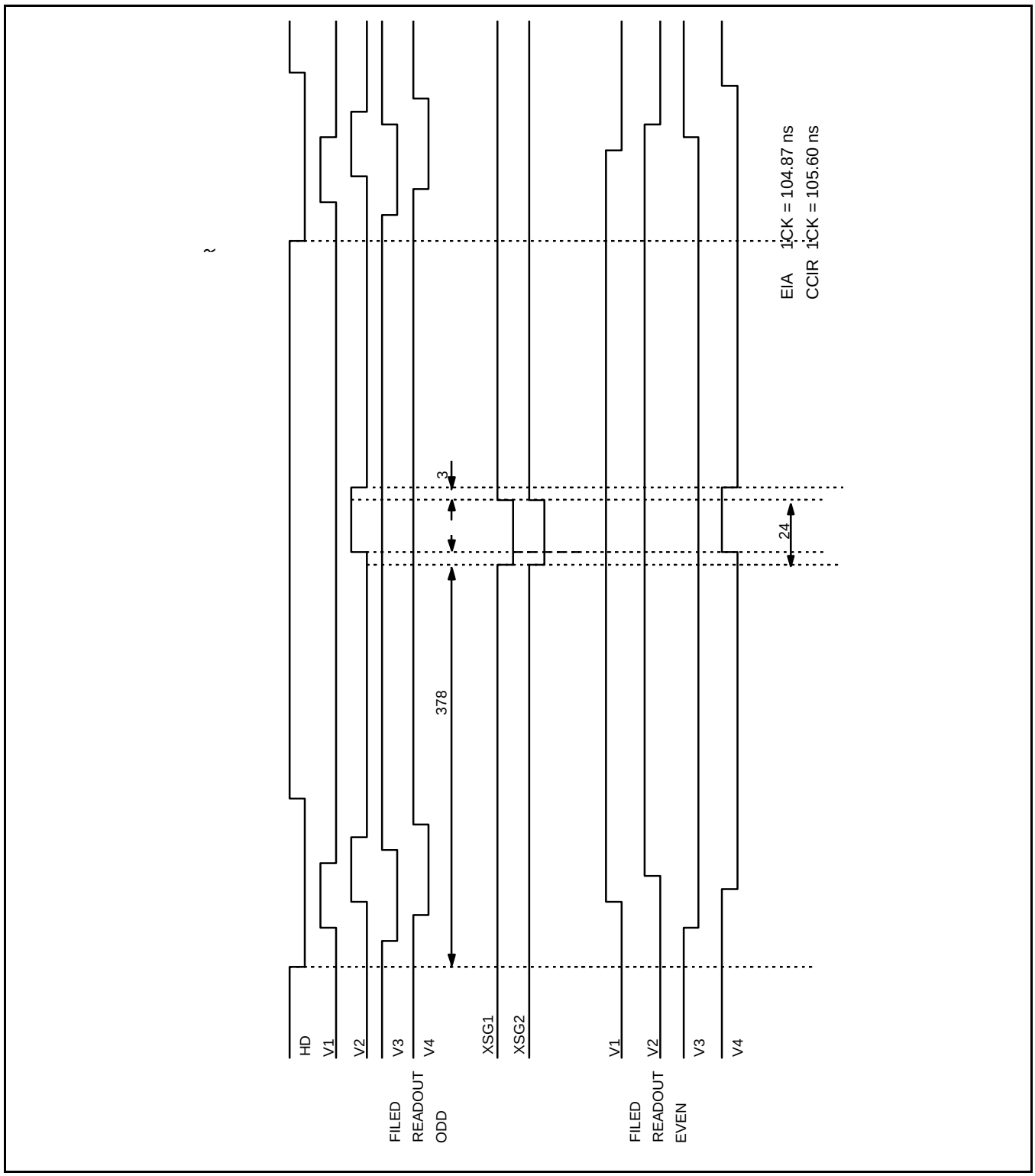


VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR NORMAL EIA AND CCIR

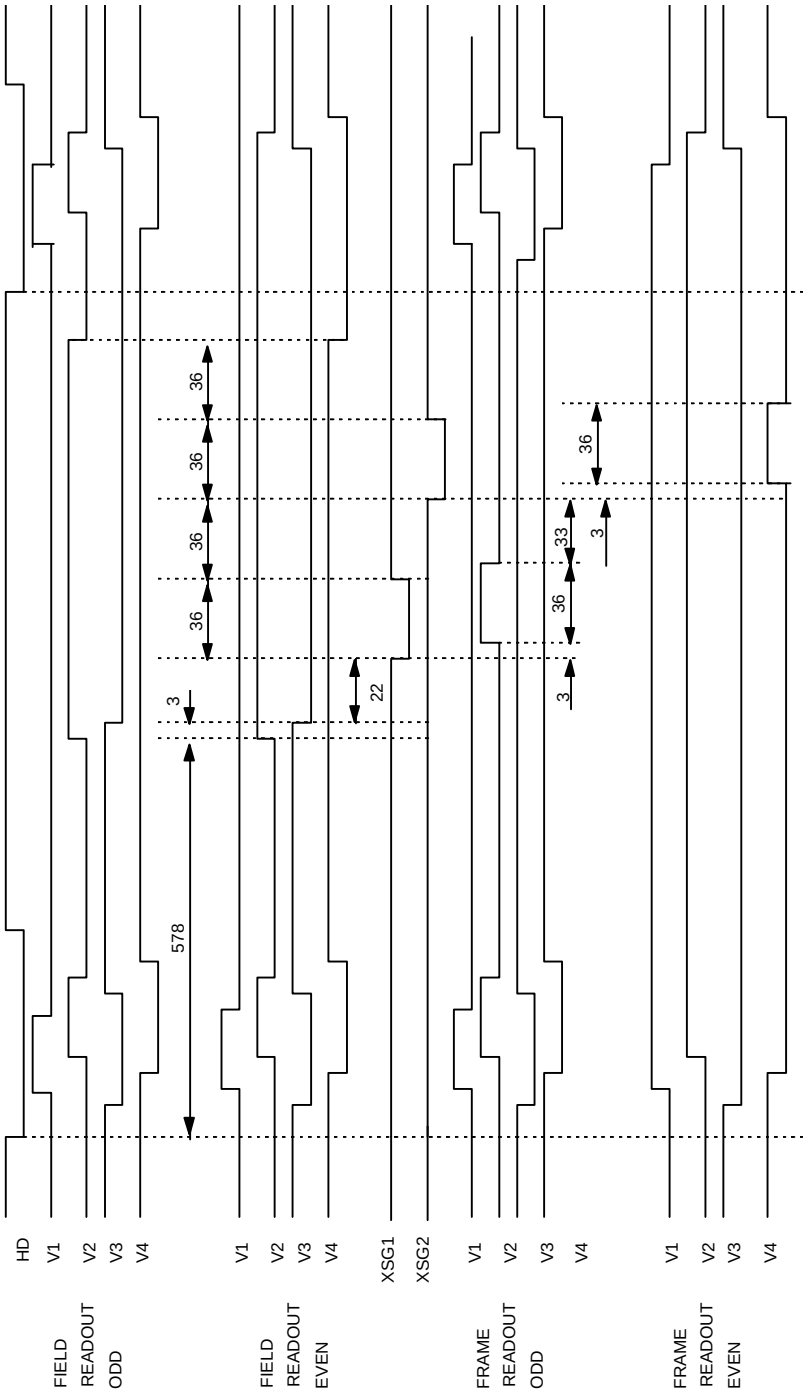


SAMSUNG ELECTRONICS

VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR NORMAL EIA AND CCIR

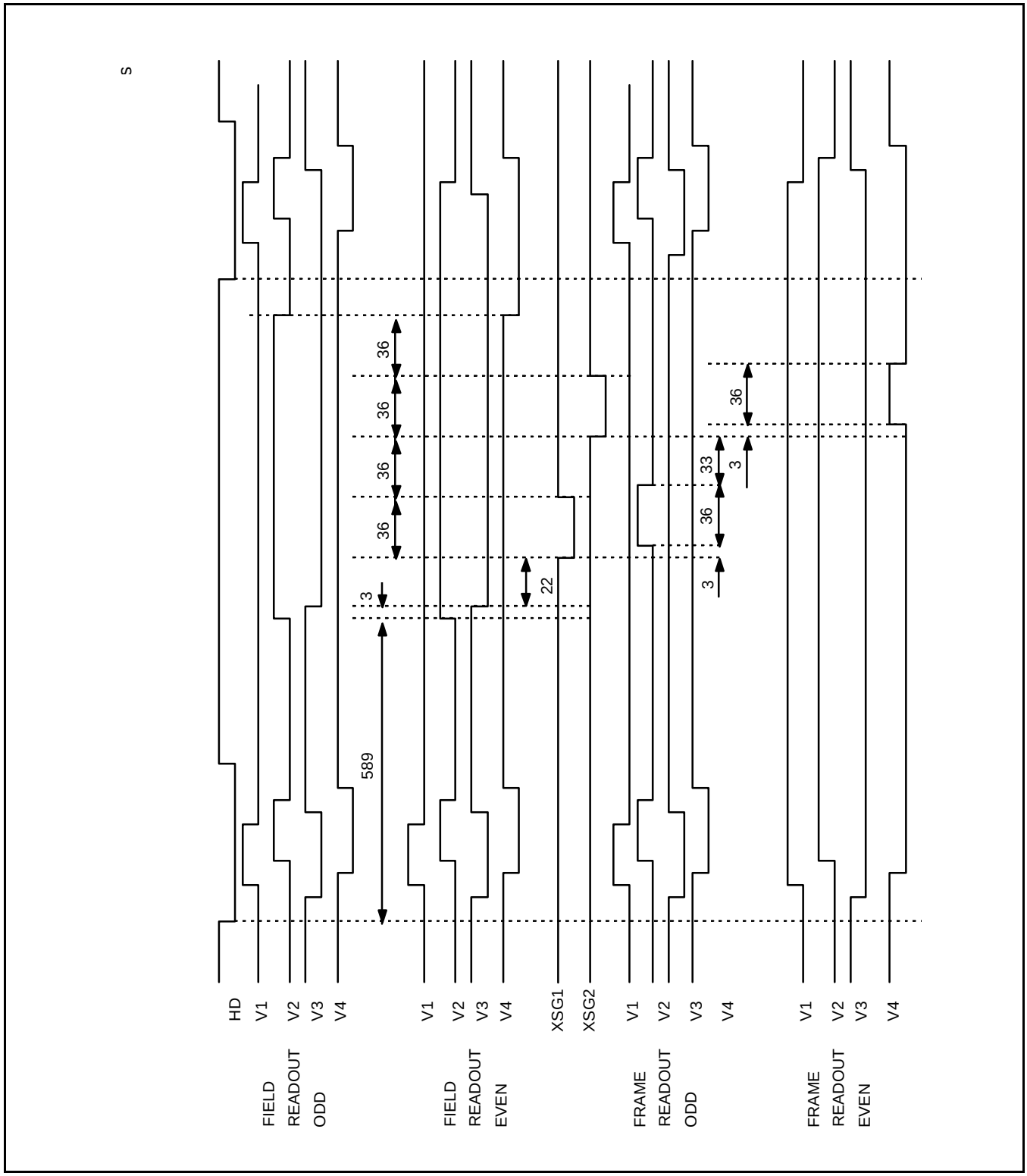


VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR Hi- 8 EIA **UNIT : 1CK = 69.84ns**

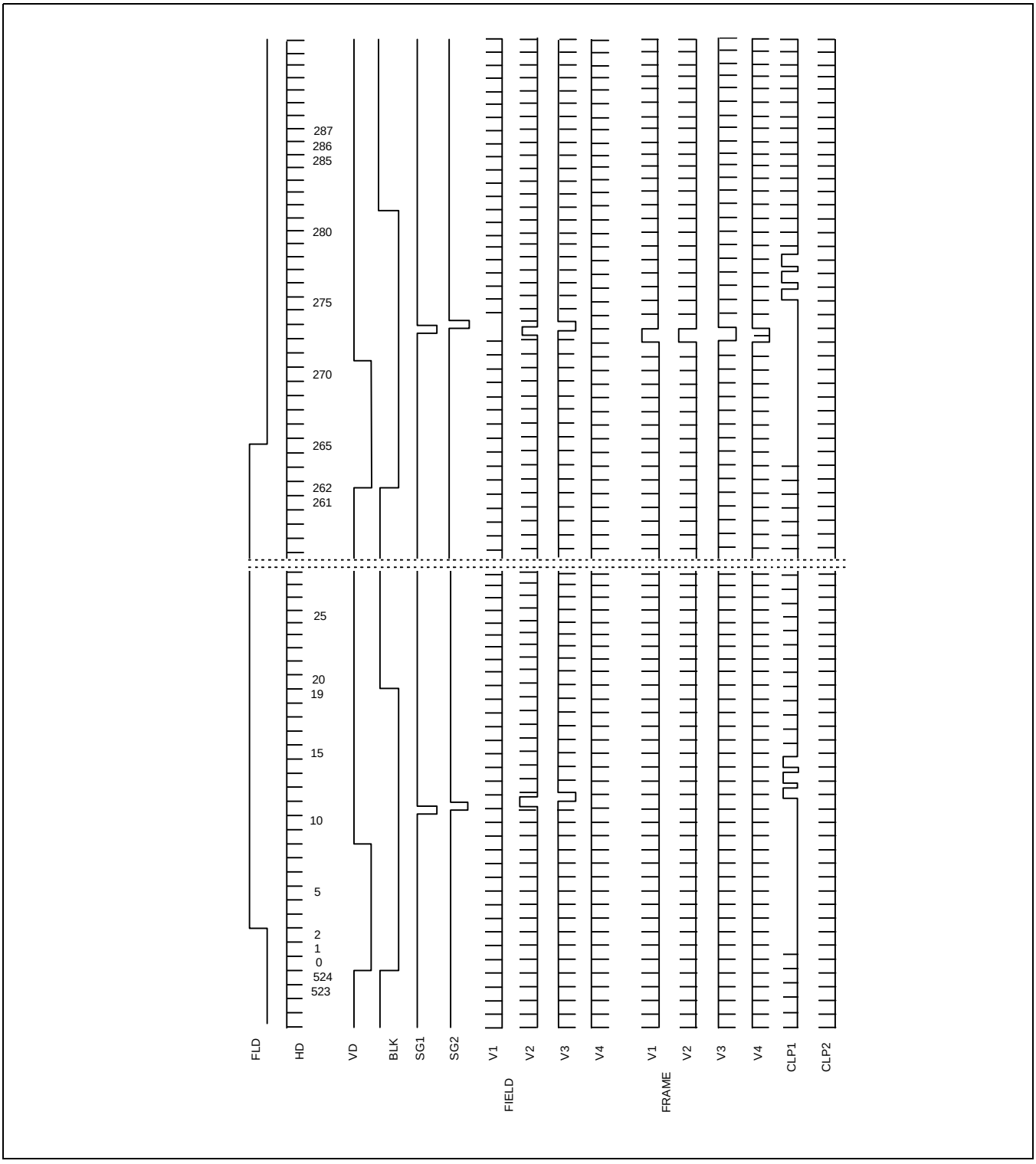


SAMSUNG ELECTRONICS

VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR Hi- 8 CCIR **UNIT : 1CK = 70.48ns**

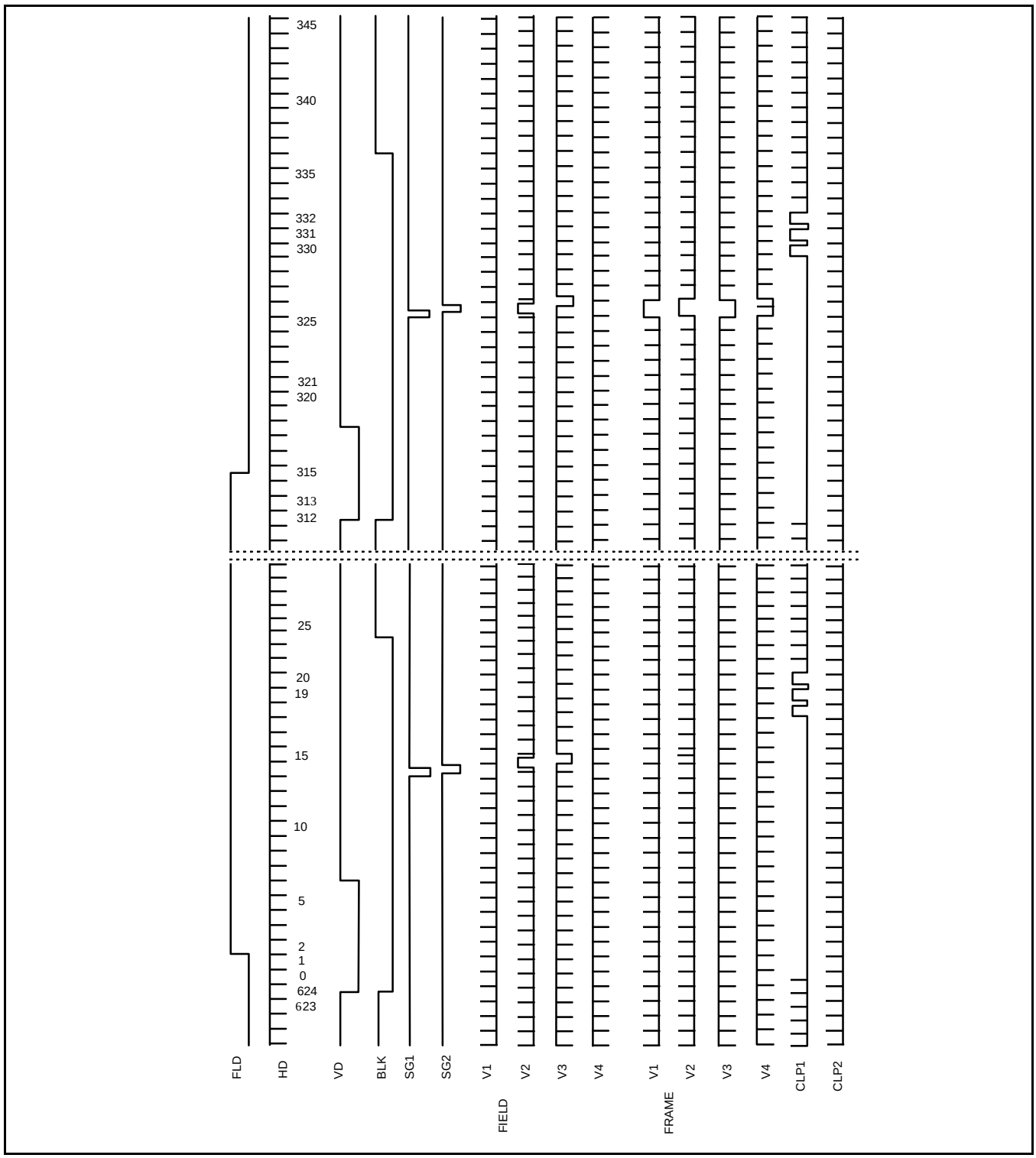


NORMAL EIA VERTICAL TIMING CHART AT INTERLACE

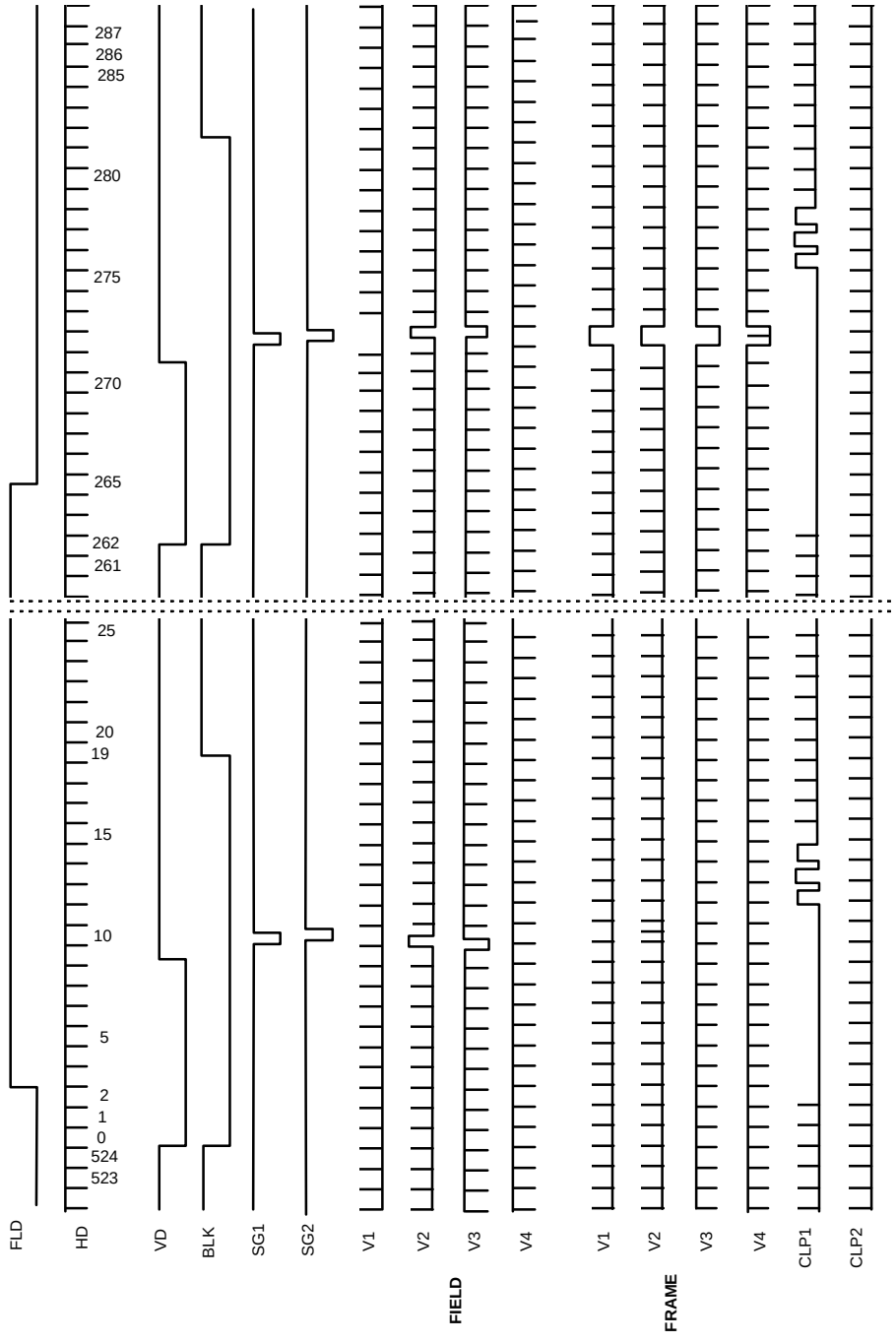


SAMSUNG ELECTRONICS

NORMAL CCIR VERTICAL TIMING CHART AT INTERLACE

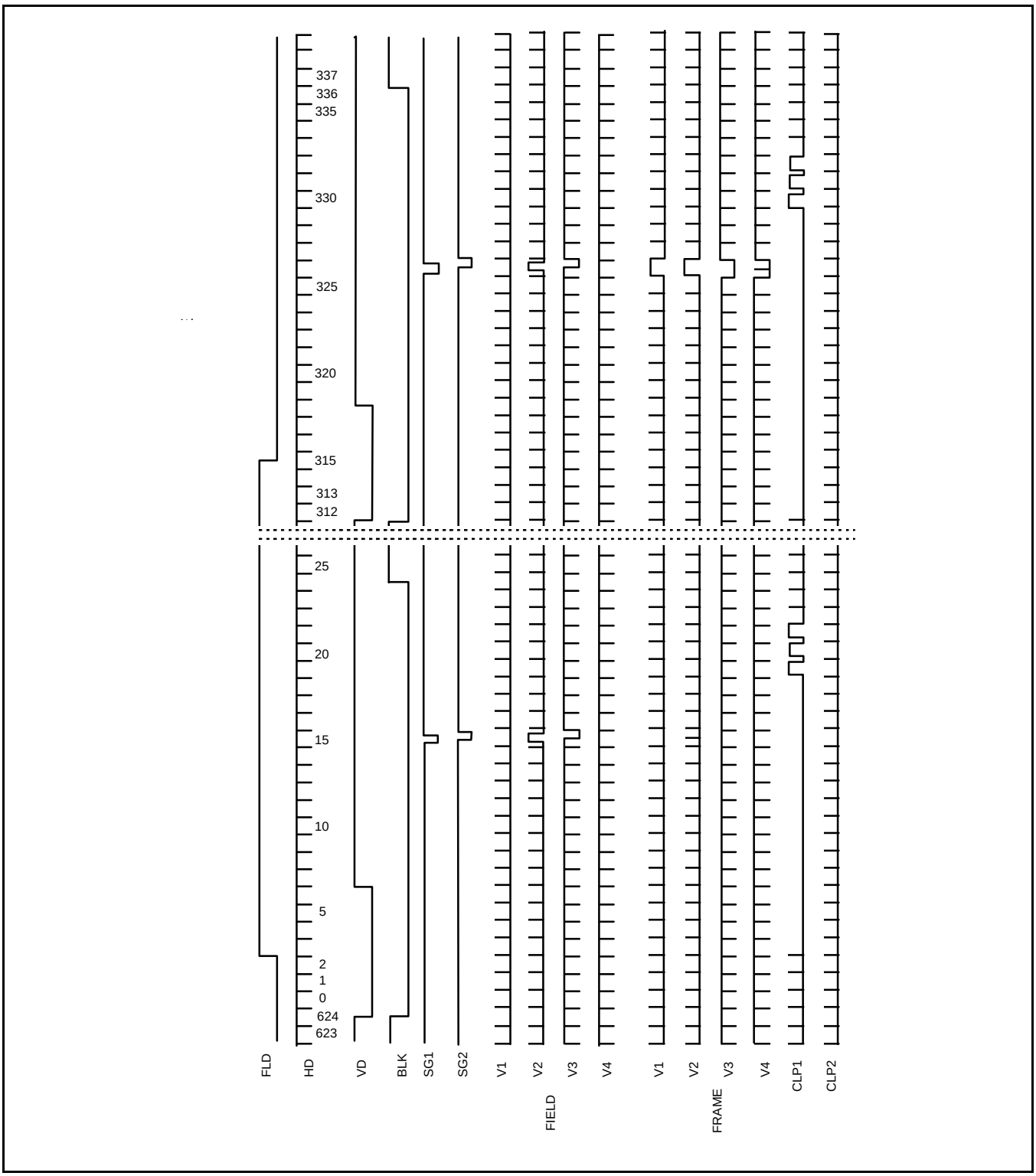


Hi- 8 EIA VERTICAL TIMING CHART AT INTERLACE

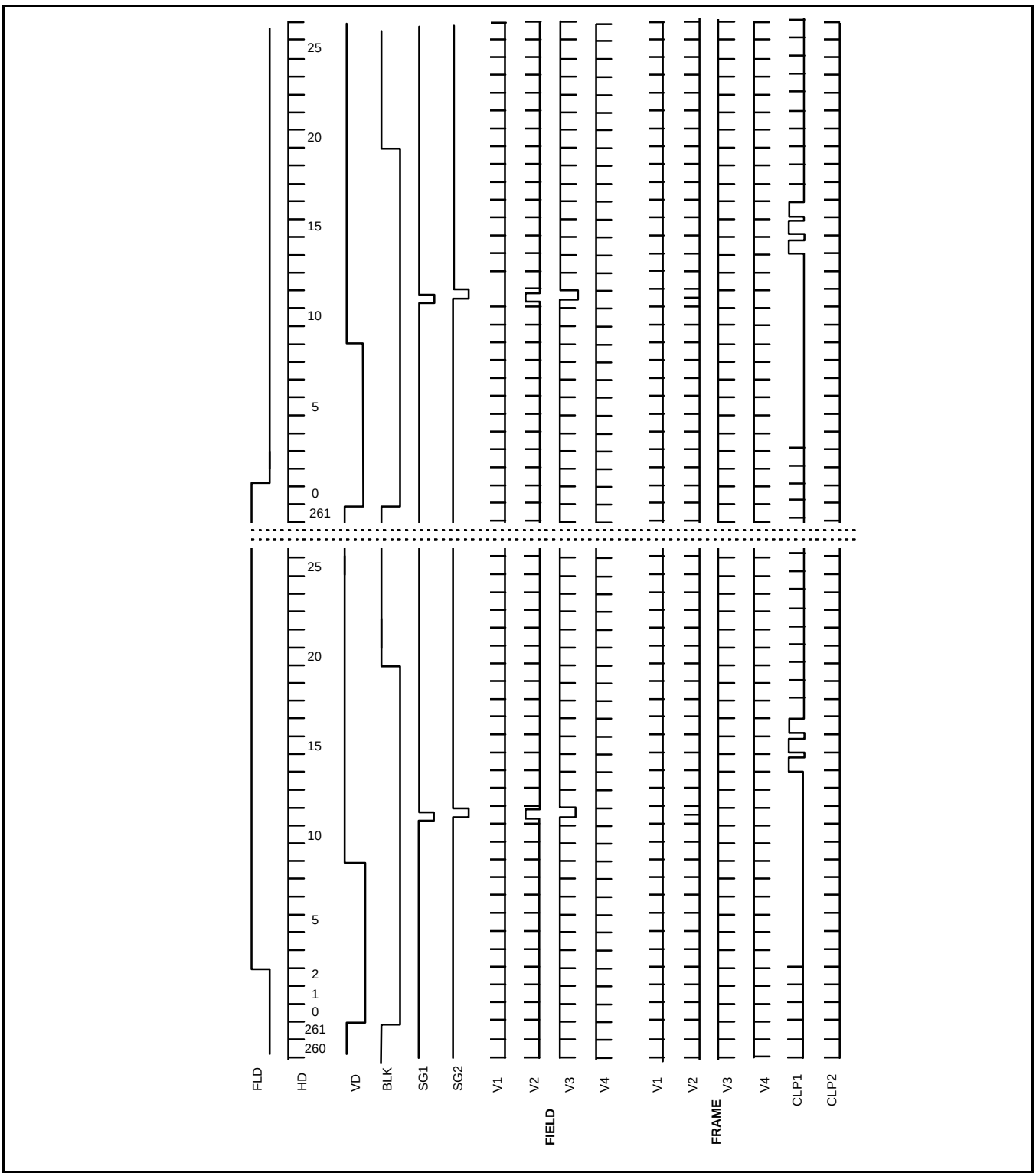


SAMSUNG ELECTRONICS

Hi- 8 CCIR VERTICAL TIMING CHART AT INTERLACE

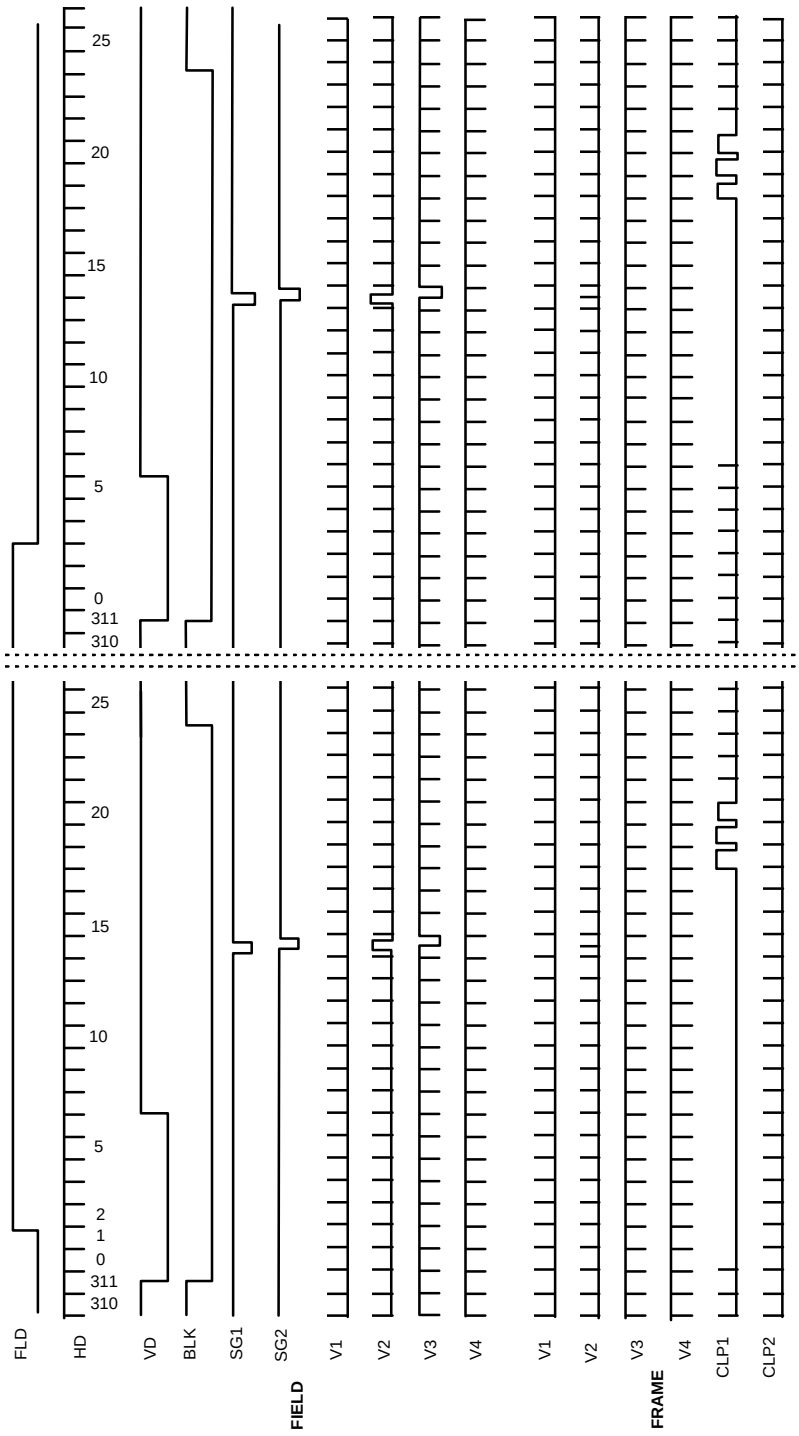


NORMAL EIA VERTICAL TIMING CHART AT NON- INTERLACE

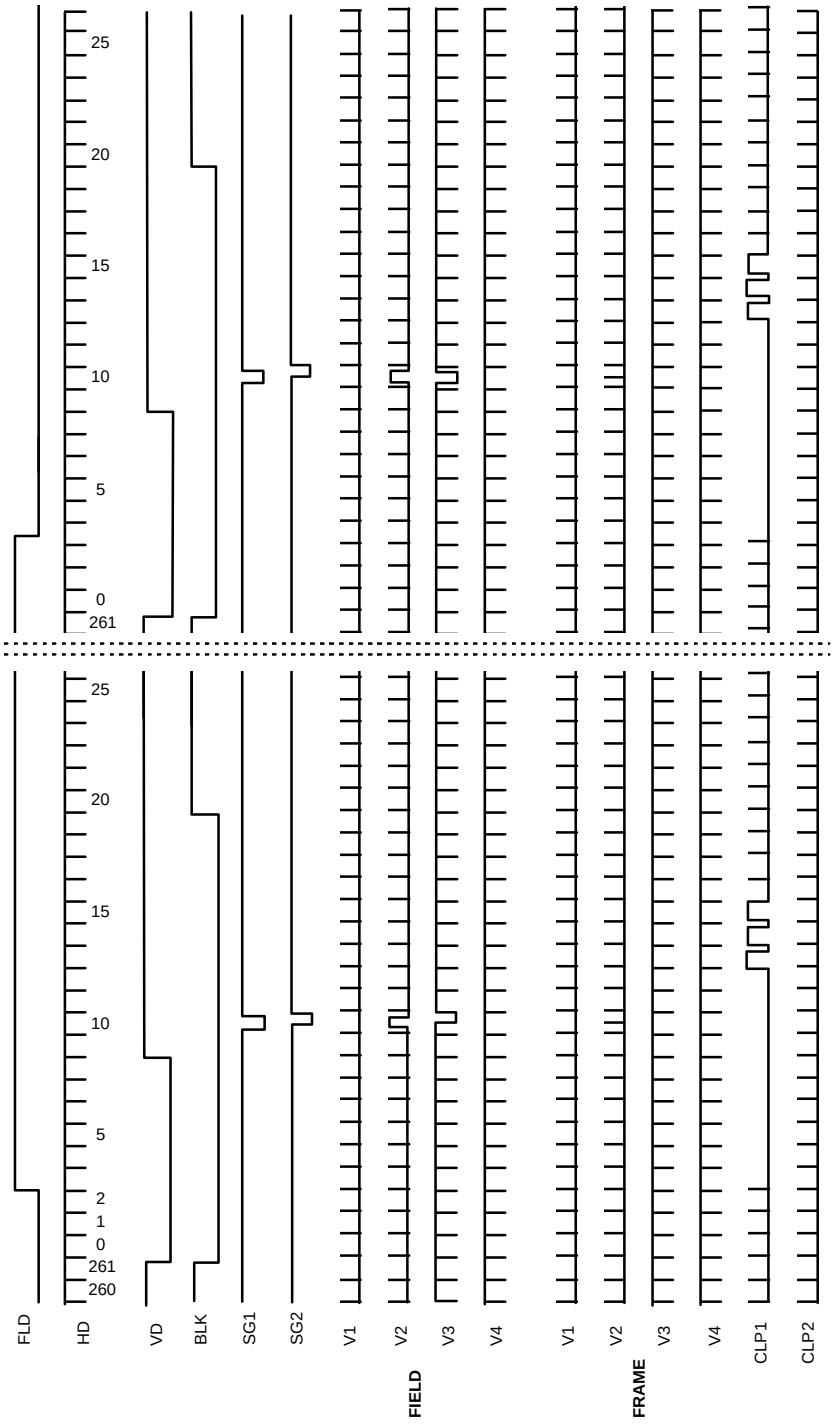


SAMSUNG ELECTRONICS

NORMAL CCIR VERTICAL TIMING CHART AT NON- INTERLACE

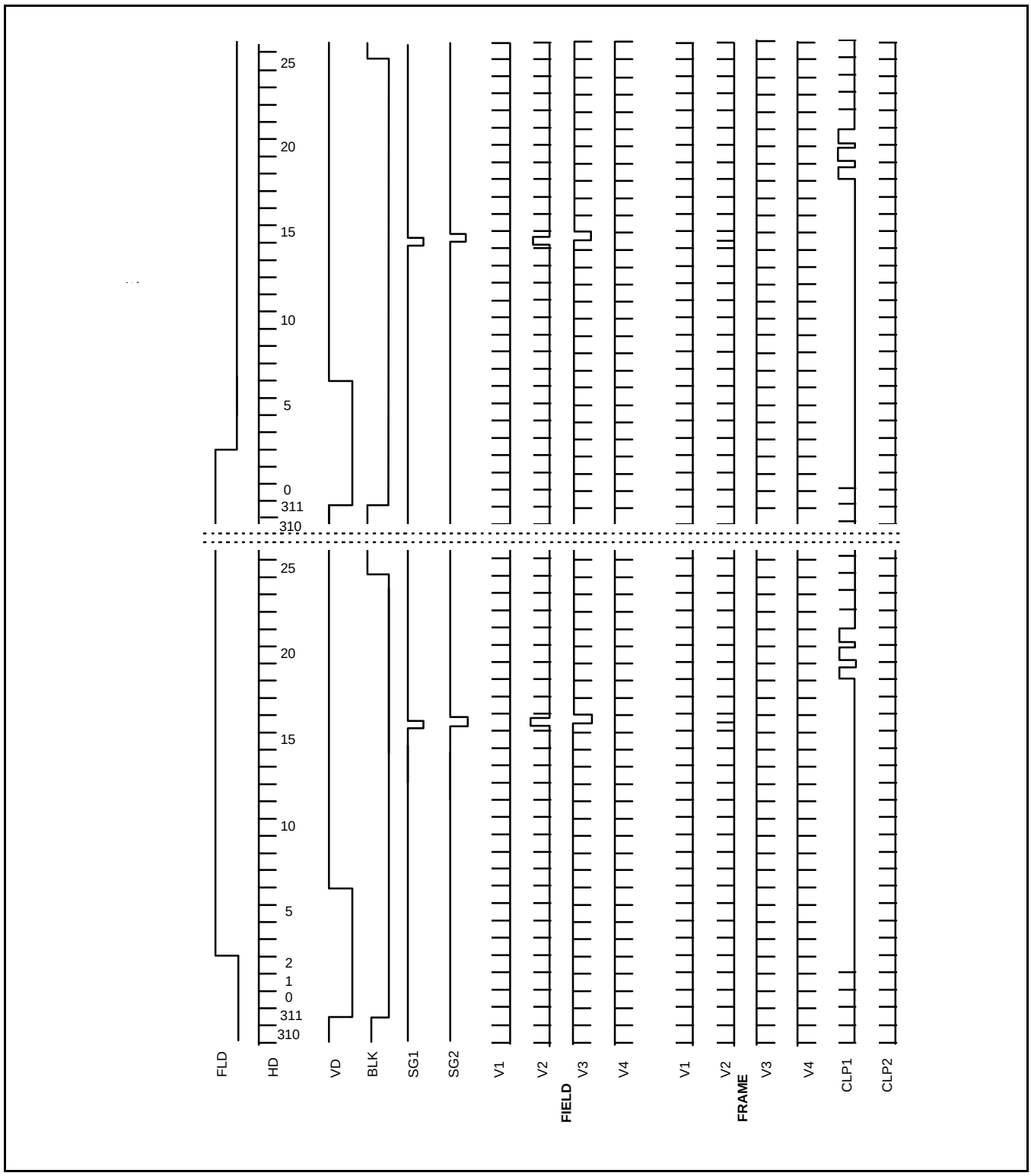


Hi- 8 EIA VERTICAL TIMING CHART AT NON- INTERLACE

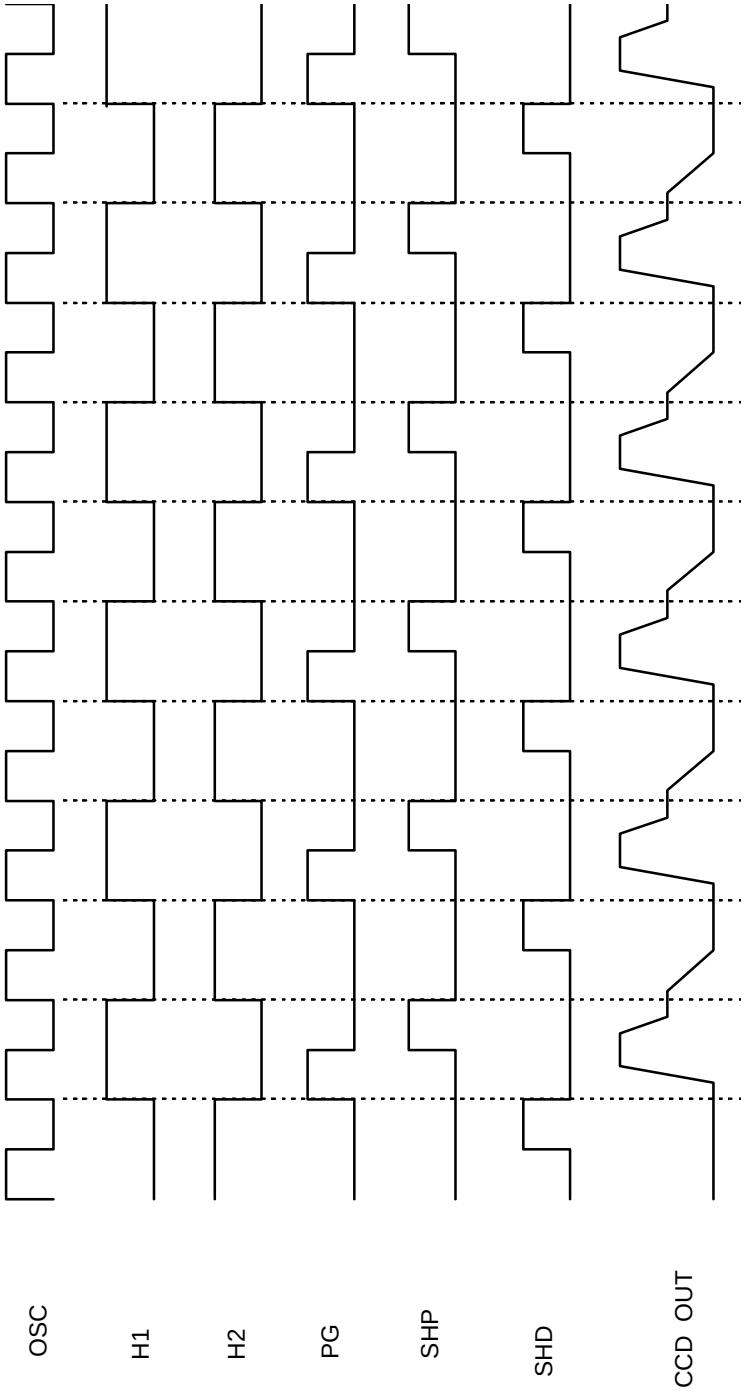


SAMSUNG ELECTRONICS

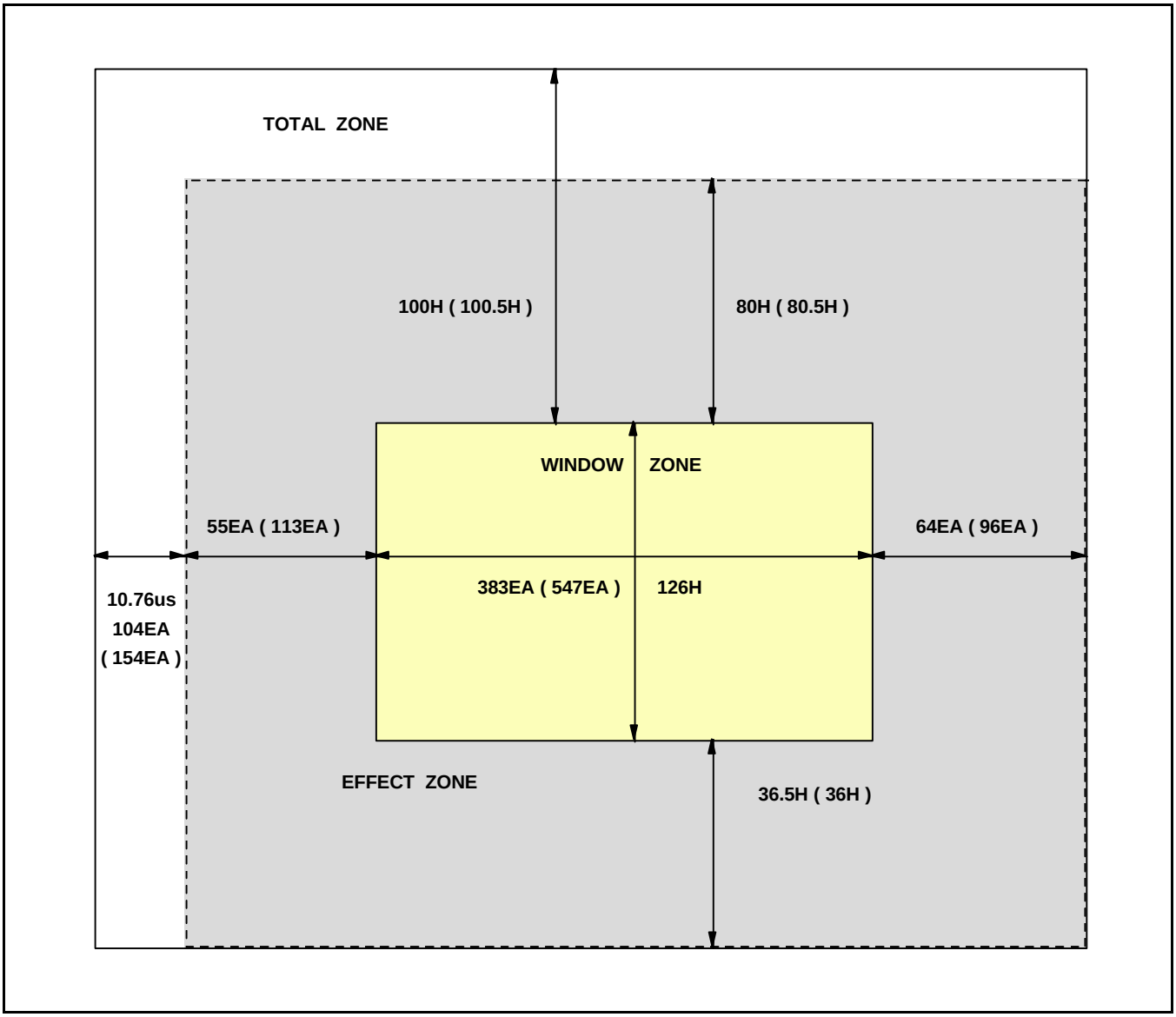
Hi- 8 CCIR VERTICAL TIMING CHART AT NON- INTERLACE



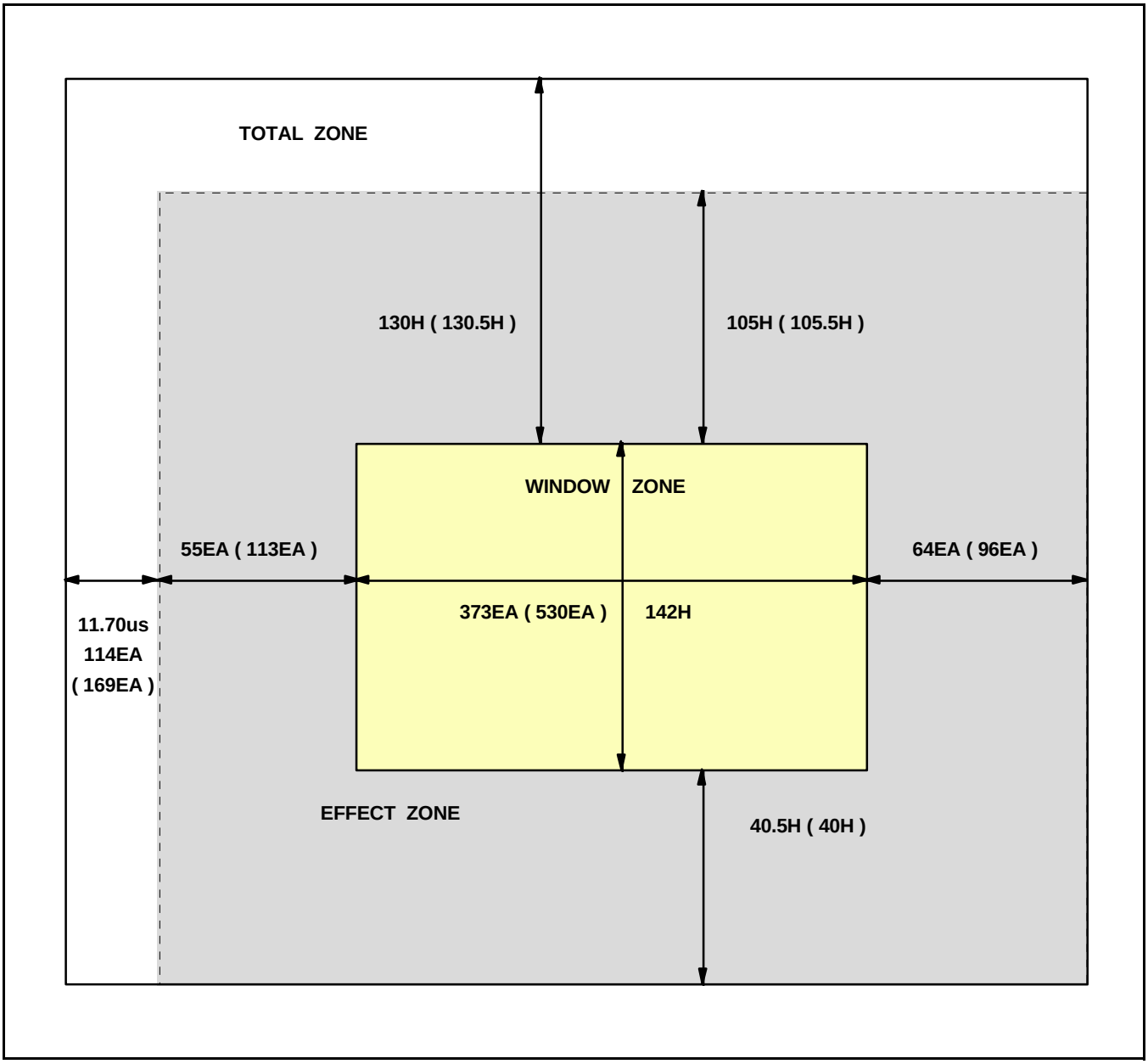
HIGH SPEED PHASE TIMING CHART



EIA NORMAL / Hi- 8 WINDOWS AREA



CCIR NORMAL / Hi- 8 WINDOWS AREA



SAMSUNG ELECTRONICS

APPLIATION EXAMPLE

(EIA NORMAL AUTO IRIS MODE APPLICATION)